Unified random access memory (URAM) by integration of a nanocrystal floating gate for nonvolatile memory and a partially depleted floating body for capacitorless 1T-DRAM

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Abstract

This paper describes a unified memory (URAM) that utilizes a nanocrystal SOI MOSFET for multi-functional applications of both nonvolatile memory (NVM) and capacitorless 1T-DRAM. By using a discrete storage node (Ag nanocrystal) as the floating gate of the NVM, high defect immunity and 2-bit/cell operation were achieved. The embedded nanocrystal NVM also showed 1T-DRAM operation (program/erase time = 100 ns) characteristics, which were realized by storing holes in the floating body of the SOI MOSFET, without requiring an external capacitor. Three-bit/cell operation was accomplished for different applications – 2-bits for nonvolatility and 1-bit for fast operation.

1. Introduction

Numerous works, both conceptual and structural, have been reported in efforts to continue the current trend of downscaling Flash memory and dynamic random access memory (DRAM). For conventional Flash memory, a key issue is the enhancement of the defect immunity, which can provide prolonged retention time and further scalability. The use of nanocrystals (NC) as a discrete storage node gives much interest to researchers in this area due to its high defect immunity, which is attained through reduced lateral charge transfer [1–5]. NCs also provide an opportunity of 2-bit/cell operation through the use of a localized charge trapping structure [6–9]. In relation to the present embedded DRAM, which consists of 1 transistor/1 capacitor (1T/1C), one of the major challenges is integrating a capacitor that sustains sufficient capacitance in a smaller cell area. A 1T-DRAM cell was proposed using a silicon-on-insulator (SOI) substrate [10–12]. This concept uses the floating body of a partially depleted (PD) SOI MOSFET as a charge storage node instead of a capacitor of an embedded DRAM. Excessive holes are generated by impact ionization and are accumulated in the lowest potential area of the floating body. The accumulated holes result in an increase of the drain current. By sensing the current difference, this structure realizes DRAM operation without an extrinsic capacitor, which would involve an additional complex capacitor-fabrication process and require cell area. In this paper, we describe a unified RAM (URAM) of NC-embedded PD SOI MOSFET that unifies multi-functional operations such as 2-bits for NVM operation and an additional 1-bit for 1T-DRAM fast operation using the aforementioned single transistor.

2. URAM fabrication

For the fabrication of the URAM, which uses Ag NCs as a floating gate, a p-type (100) SOI wafer was initially prepared. The SOI and buried oxide (BOX) thickness are 100 nm and 370 nm, respectively. The device active area was defined by mesa etch using TMAH (25%) for cell isolation and a N+ source/drain junction was formed by implanting phosphorus with a patterned photore sist. The undoped 100-nm-thick SOI will become a PD body as a charge storage node for the 1T-DRAM operation. After standard cleaning, a 5-nm-thick tunneling oxide layer was thermally grown at 850 °C. Ag NCs by thermal decomposition method [5] were used for the charge storage node of the Flash memory. The details of formation of Ag NCs have been reported elsewhere [5].
dielectrics. A competitively thick HfO2 (30 nm) control layer was deposited as a control dielectric and aluminum was deposited for the gate electrode.

A circuit symbol of a URAM, which performs both NVM and 1T-DRAM operations, is depicted in Fig. 1a. The 3-dimensional schematic of URAM (Fig. 1b) shows two separate charge storage regions – the NC floating gate and the floating body. The use of a NC floating gate offers two advantages compared to the use of a polycrystalline silicon layer in conventional Flash memory. The first is that it alleviates the limit of downscaling of conventional Flash memory by improving the defect immunity. The other is that it allows implementation of 2-bit/cell operation through localized charge distribution by channel hot electron injection (CHEI). With 2-bit/cell operation using a NC floating gate, there is a hidden bit that uses the floating body for an 1T-DRAM operation. By impact ionization, excessive holes are accumulated in the floating body of the PDSOI. Using this phenomenon, the floating body serves as a second charge storage node. Fig. 2 shows a transmission electron microscopy (TEM) image of the fabricated Ag NC-embedded URAM and a scanned electron microscopy (SEM) image of embedded Ag NCs.

3. Device characteristics and discussion

Fig. 3 shows current–voltage ($I_{DS}$–$V_{GS}$) characteristics and retention characteristics for multi-bit/cell operation using the localized charge trap node by CHEI as the NVM operation. The dashed lines are the initial $I_{DS}$–$V_{GS}$ from a fresh device at both directions (reverse from drain to source and forward from source to drain). The two dashed curves are almost identical. After programming ($V_{GS}$–$V_{th}$ = 10 V, $V_{DS}$ = 5 V), a threshold voltage ($V_{th}$) difference ($\Delta V_{th}$ = 1.1 V) was observed according to the sweeping direction as shown in Fig. 3a. By the CHEI program mechanism with positive drain voltage, the energetic electrons are stored in the Ag NCs near the drain-side. The drain-side potential barrier, which is raised by the stored electrons at the drain-side, is easily lowered by a drain induced barrier lowering effect (DIBL) at the forward mode. However, when the sweeping direction is changed from forward to reverse, the lowering of drain-side potential barrier is less effective than that of forward read direction, and thus the $V_{th}$ at the forward reading mode is lower than that at the reversed reading mode. By sensing the polarity of this $V_{th}$ difference, it is possible to differentiate between the bit 1 and bit 2 regions. For each read direction, the retention time characteristics of a NVM mode with $W/L = 10 \mu m/5 \mu m$ were measured at room temperature as shown in Fig. 3b. Comparing $\Delta V_{th}$ = 1.34 V after 10 years for 1-bit operation of the NVM mode, the reverse read of the 2-bit operation has 50% deviation of the stored charges at $10^7$ s. The poor retention characteristic needs to be improved for the multi-bit URAM application. Recently bandgap-engineering concept was introduced to...
enhance the charge storability as well as P/E efficiency [13,14]. This concept can be applicable to the URAM structure.

Fig. 4 shows program/erase (P/E) conditions and retention characteristics at the reading mode for 1T-DRAM operation. The applied P/E pulse width was 100 ns. After programming with a pulse of $V_{GS} = 2.5$ V (>$1.12$ $V (E_g/q)$ at 300 K, silicon bandgap ($E_g$)), $V_{GS}$ (front gate bias) = 1.5 V, and $V_{BG}$ (back gate bias) = −30 V, excessive holes are generated by impact ionization and stored in the floating body. This leads to decrement of $V_{th}$, which places the source current ($I_{SD}$) in a “1” state. In order to erase the stored holes regarded as a ‘0’ state, forward bias between the body and drain ($V_{DS} = −1$ V) is applied, and the stored holes are then swept out of the floating body. $I_{SD}$ is decreased due to the raised $V_{th}$. Sensing the difference of the source current (Δ$I_{SD}$) provides information as to whether holes exist. As a result, the two states of ‘1’ and ‘0’ can be distinguished. The inset of Fig. 4 shows the retention characteristic at the reading mode. The accumulated holes are maintained for 180 ms with 8 μA sensing window.

To operate the device for simultaneous NVM and 1T-DRAM operation with a single transistor cell, the operations should not disturb each other. Fig. 5 represents the available operation domain for each operation. In the 1T-DRAM operation domain ($|V_{GS}| ≤ 4$ V), $I_{SD}$−$V_{GS}$ hysteresis does not appear. This means that the current change shown in Fig. 4 solely originates from the hole charging in the floating body of the PSDOI. The other domain ($|V_{GS}| ≥ 4$ V) is defined for NVM operation. Thus, the two operations are clearly differentiated by the bias condition.

4. Conclusions

Both operations of 2-bit NVM and 1T-DRAM were demonstrated with only a single transistor of a NC-embedded SOI MOSFET using two different storage nodes – nanocrystals for 2-bit nonvolatility of NVM and the floating body for fast operation of 1T-DRAM. Due to the possibility of high bit density using the current technology node without aggressive further scaling, the proposed device structure holds considerable promise for future applications and is expected to be a driver of the future semiconductor industry.

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Appendix A. Supplementary material

Supplementary data associated with this article can be found, in the online version, at doi:10.1016/j.sse.2009.01.015.

References