One-Transistor Nonvolatile SRAM (ONSRAM) on Silicon Nanowire SONOS
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Abstract
A one-transistor nonvolatile SRAM (ONSRAM) on a silicon nanowire (SiNW) SONOS is demonstrated. A nonvolatile memory (NVM) property is attained by employment of O/N/O gate dielectric stacks as an electron storage node, and SRAM functionality is achieved by exploiting latch phenomena of a floating body in SiNW. Abrupt inverter switching, superior sensing current (≥ 21µA), and robust interference immunity between SRAM and NVM verify the feasibility for the suggested ONSRAM.

Introduction
A partially-depleted (PD) FinFET was reported to enhance 1T-DRAM performance [1,2]; however it imposes a constraint on further scaling due to the tradeoff relation between the sensing margin and immunity to short-channel-effects (SCEs), as shown in Fig. 1. Recently, a bipolar-junction-transistor (BJT)-based 1T-DRAM demonstrated that a fully-depleted (FD) device can perform bi-stable memory operation with a wide sensing window and long data retention without a floating body region in PDSOI [3,4]. The latch-up caused by positive feedback on the parasitic BJT, which is normally an undesired phenomenon, displays a hysteresis loop with a steep subthreshold slope (SS), similar to impact–ionization metal-oxide-semiconductor transistors (I-MOS) [5] and tunneling field-effect transistors (TFET) [6]. These features can be explored for use in single transistor based SRAM operation [7]. In the present work, we demonstrate SRAM function in a single silicon nanowire (SiNW) MOSFET that has high SCEs immunity and propose a one-transistor nonvolatile SRAM (ONSRAM) for device-level fusion through the use of O/N/O layers as a floating gate and gate dielectrics, as illustrated in Fig. 2. A single ONSRAM chip to embody the one-transistor (1T) SRAM can replace a multi-chip-package (MCP) to stack SRAM as buffer memory and flash memory for low power, compact mobile electronic devices.

Device Fabrication
The process flow and photographs of the SiNW SONOS are illustrated in Fig. 3. The top silicon layer, having a thickness of 110 nm, in a silicon-on-insulator (SOI) wafer was thinned to 50 nm via oxidation and a wet-etch process. After delineation of the photoresist with 150-nm-line width, the photoresist was partially trimmed to 50 nm through an O2 plasma ashing process. A 50-nm-width and -height top silicon was patterned and reduced to 30 nm by the thinning process. O/N/O of 3nm/7nm/12nm and n+ in-situ poly-Si layers were stacked sequentially and patterned simultaneously. Finally, S/D was formed by an implantation and activation process. 150 nm-long- and 50 nm-thick-devices were nominally used for the measurement.

Results and Discussion
A. NVM characteristics
Despite a thick gate dielectric, the SiNW SONOS shows comparable program efficiency by a channel-hot-electron-injection (CHEI) mechanism and a steeper subthreshold slope (SS) due to high gate controllability as compared to a PD FinFET SONOS, as shown in Fig. 4. Full program and erase (P/E) were achieved at V G, PGM=11V and V G, ERS=-12V with a duration of 80 µsec at V D,PGM=4V and V D,ERS=4.5V, respectively. Acceptable charge retainability (∆Vth=3.3V @ 10 year) was attained for the SiNW SONOS with an endurance characteristic of over 10⁵ P/E cycles, as shown in Fig. 5.

B. SRAM characteristics
The bistable hysteresis and steep SS less than 20mV/dec were attributed to iterative impact ionization, which results in activation of a parasitic npn BJT. Current is thereby multiplied by a positive feedback loop, as illustrated in Fig. 6 [8]. To set up SRAM operation conditions, the latch-up voltage is examined for various V DS and V GS, as shown in Fig. 7. The parameter instability with respect to V D is shown in Fig. 8. Depending on V DS, less V th degradation and steeper SS were achieved for the thinner d NW despite...
narrower hysteresis. The trade-off between the hysteresis window and SS as well as $V_{th}$ should be considered in designing the cell architecture, particularly in terms of scalability and operation window. Fig. 9 shows the operational timing diagram with 5nsec P/E pulses; the measured current of the SiNW device is 3 times larger at the “1” state and smaller at the “0” state relative to the PDSOI FinFET. This indicates that sensing window is significantly improved at the SiNW device. The static latch by avalanche multiplication through positive feedback assures no data loss, a feature that can be applicable for 1T-SRAM, as shown in Fig. 10. According to the statistical analysis, sensing current larger than 21µA is achieved, as shown in Fig. 11. Once the parasitic BJT is triggered and holes are charged in the p-type floating body, i.e. the base of BJT, pre-stored data are sustained in the stand-by (hold) state by $V_G = -2.5V$ and floating body, parasitic BJT is triggered and holes are charged in the p-type larger than 21µA is achieved, as shown in Fig. 11. No $V_{th}$ shift was found in either AC or DC stress tests.

In order to support functionality of a 1T-SRAM architecture, the voltage transfer characteristic of a SiNW inverter loaded by a pull-up resistor (see the inset of Fig. 14) was investigated, as shown in Fig. 14. Abrupt switching ensures the superiority of ONSRAM for ultra-scaled SRAM in terms of noise margin as well as data retainability. Fig. 15 presents a cell array diagram for ONSRAM. For a 1T-SRAM mode in ONSRAM, the cells are read through a selected row and column lines (RL and CL). Programming is accomplished by inducing BJT current multiplication through biasing of the write row line (WR) and CL. Forward junction current at the RL erases the cells by unlatching them. With regard to a disturbance issue, gate- and drain-disturbances are characterized in Fig. 15(b) and revealed to be of no significance, because the operation regime of SRAM is in accumulation or depletion. ONSRAM is capable of dynamic allocation of storage capacity according to the customized functionality for each part of SRAM and NVM without an additional chip (Fig. 16(a)). Additionally, ONSRAM normally can operate at SRAM mode for fast data access and retain nonvolatile data at NVM mode for nonvolatile data backup. Moreover, ONSRAM implemented in a single transistor is able to recall data even during a power-off. The corresponding sequences are depicted in Fig. 16(b).

Conclusions

A novel ONSRAM architecture that enables multi-functionality of SRAM and NVM was demonstrated in a single cell, and its operation scheme was presented. ONSRAM was implemented on a silicon nanowire embedded single transistor with employment of the SONOS structure. The proposed ultra-scalable hybrid ONSRAM, which did not show interference between SRAM and NVM, is expected to replace package based hybrid memory in a system-on-chip (SoC) and MCP.

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References

Fig. 1 (a) Cross-sectional TEM image of three-dimensional PDSOI FinFET. (b) IT-DRAM sensing margin and (c) SS dependency on Hg. PD region plays a role of hole storage nodes. Despite the high IT-DRAM sensing margin for low Hg device, it suffers from 500 SCEs when it is scaling down.

Fig. 2 (a) SiNW SONOS schematic and (b) circuit symbol of ONSRAM.

Fig. 3 (a) Process flow of SiNW SONOS. Bird’s eye views of SEM (b) after the trimming process and (c) after device fabrication. (d) Cross sectional TEM image along x-x’ direction in Fig. 3(c) and (e) TEM image of O/N/O stacks. The gate fully surrounds the silicon nanowire.

Fig. 4 I_DS-VGS characteristics for NVM programming operation of SiNW SONOS and PDSOI FinFET SONOS.

Fig. 5 (a) Retention and (b) cyclic endurance comparison between SiNW SONOS and PDSOI FinFET SONOS. SiNW shows enhanced charge stability relative to the FinFET. For both structures, ΔVth is sustained even after 10^5 P/E cycles.

Fig. 6 (a) Measured nominal I_DS-VGS characteristics showing single transistor latch effects in the form of the steep slope and hysteresis.

Fig. 7 (a) I_DS transfer and (b) I_DS-VDS output characteristics according to V_DS and V_DS bias. Conditions for SRAM operation were optimized by virtues of these two characteristics.
A narrow dNW device shows less Vth lowering and steeper SS. However, it sacrifices sensing window.

The SiNW achieves excellent charge retainability due to its non-destructive read operation by latch.

The soft programming effects are negligible for the SRAM operation of the SiNW device.

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