A thickness modulation effect of HfO₂ interfacial layer between double-stacked Ag nanocrystals for nonvolatile memory device applications

Seong-Wan Ryu and Yang-Kyu Choi

Department of Electrical Engineering and Computer Sciences, Korea Advanced Institute of Science and Technology, Daejeon 305-701, Republic of Korea

Chan Bin Mo, Soon Hyung Hong, Pan Kwi Park, and Sang-Won Kang

Department of Material Science and Technology, Korea Advanced Institute of Science and Technology, Daejeon 305-701, Republic of Korea

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This paper presents a detailed study on the effect of different thicknesses of HfO₂ high-k interfacial layer between double-stacked layers of Ag nanocrystals formed by a chemical synthesis and thermal decomposition method. To confirm the formation and purity of the well-ordered Ag nanocrystals with a high density (2.7 \times 10^{12} \text{ cm}^{-2}), transmission electron microscopy and x-ray diffraction analysis were used. After fabricating metal-oxide-silicon structures with 2 and 6 nm interfacial HfO₂ and the double-stacked Ag nanocrystals, a program efficiency and retention time characteristics were investigated. © 2007 American Institute of Physics. [DOI: 10.1063/1.2430785]

A conventional nonvolatile memory (NVM) with a continuous polysilicon layer called a floating gate has a scaling limit below the 45 nm technology node, because the retention property degrades as the tunneling oxide thins out. Thus, researchers have introduced a NVM concept by using discrete storage nodes with high immunity to oxide defects. Since the introduction of a nanocrystal (NC) NVM, various NC materials have been widely studied, such as silicon and metal oxide and metal. Of these, metal NCs are highly recommended for high programming efficiency and prolonged retention time by the high density of states and work function engineering, despite their incompatibility with conventional silicon processes.

A major method of metal NC formation has been to use a self-assembled NC formation technique. According to the technique, it is hard to control the size and space of the NCs at the same time. To achieve uniform NCs' size and distribution is crucial for application to the NC nonvolatile memory devices beyond the 45 nm technology node because a uniformity of device performances such as a threshold voltage and retention time is sensitive to the size and distribution. Thus, a different approach, a chemical synthesis and thermal decomposition is proposed to make more uniform NCs' size and distribution. The NCs' size and NC-to-NC space are able to be controlled individually. The NCs' size is controlled by a size-selective precipitation technique and the NC-to-NC space is controlled by the length of self-assembled monolayer surrounding the nanocrystal in the chemical synthesis and thermal decomposition method. Recent reports indicated that a structure which uses double-stacked NC (DSNC) layers achieves a wide memory window and an enhanced retention time. Therefore, it was studied for improved nonvolatile memory characteristics by using thermally decomposed Ag NCs (work function=5.1 eV).

The thickness modulation effect of the interfacial dielectric, inserted between the double-stacked Ag NC layers, will be discussed.

Metal-oxide-silicon (MOS) structures were fabricated on a p-type (100) silicon wafer. After a standard cleaning, 4.5 nm tunneling oxide was thermally grown at 850 °C for 9 min. To synthesize the Ag NCs, a mixture of a 5 mM of AgNO₃, 100 ml of oleylamine, and 6 mM of oleic acid was refluxed at 130 °C for 3 h. The size and density of the thermally decomposed Ag NCs were controlled by a size-selective precipitation technique. The Ag NCs by thermal decomposition were spin coated at 4500 rpm for 30 s on the tunneling oxide. In addition, a transmission electron microscopy (TEM) was used to get images, as shown in Fig. 1, of two different sizes of Ag NCs. The density was 2.7 \times 10^{12} \text{ cm}^{-2} for a diameter of 3–5 nm (d_{\text{avg}}=4 \text{ nm}) and 7.9 \times 10^{11} \text{ cm}^{-2} for a diameter of 5–8 nm (d_{\text{avg}}=6.5 \text{ nm}). The crystal structure of the Ag NCs was identified by x-ray diffraction (XRD) analysis and Fig. 1(c) shows that the main peaks matched those of pure metallic face-centered-cubic (fcc) Ag. For a better program/erase (P/E) efficiency, HfO₂ was used as an interfacial layer instead of SiO₂ because the energy barrier of HfO₂ (\Phi_{B}=\Phi_{E,C,HfO₂}-\Phi_{E,C,\text{Si}}=1.5 \text{ eV}) is lower than that of SiO₂ (\Phi_{B}=\Phi_{E,C,\text{Si}}=3.1 \text{ eV}). To investigate the interfacial thickness effect, HfO₂ thicknesses were split to 2 and 6 nm. The HfO₂ layer was deposited by plasma-enhanced atomic layer deposition using a Hf[N(CH₃)₂C₃H₅]₄ as a hafnium precursor and oxygen plasma as an oxidant in order to control the film thickness precisely and to insulate the Ag NCs conformally. To make DSNCs, the second Ag NC layer was spin coated on the interfacial HfO₂ under the same spin-coating conditions. A 23 nm oxide layer was deposited by using plasma-enhanced chemical vapor deposition as a control dielectric. Next, a rf magnetron sputter method was used to deposit aluminum, which was patterned for a gate electrode. Finally, a forming-gas anneal was performed at 400 °C for 30 min. The thicknesses of previously grown
SiO$_2$ and HfO$_2$ film were monitored by a spectroscopic ellipsometry. Two control groups were prepared by fabricating embedded MOS structures: the first group was used to check the shift of flatband voltage by gate dielectric layers without Ag NCs consisted of 4.5 nm tunneling oxide/6 nm HfO$_2$/23 nm control oxide/Al gate; the second group was used to investigate the effect of double-stacked Ag NCs, consisted of 4.5 nm tunneling oxide/single-stacked NCs (SSNCs)/23 nm control oxide/Al gate. For all samples fabricated and measured in this paper, the NCs of density = 2.7 $\times$ 10$^{12}$ cm$^{-2}$ and $d_{\text{avg}}$ = 4 nm were used.

To confirm the NVM operation of Ag NCs and to investigate the modulation effect of the interfacial HfO$_2$ thickness, the high-frequency (1 MHz) capacitance-voltage characteristics were analyzed. Figure 2 shows the capacitance characteristics with the shift of flatband voltage for various ranges of the gate voltage in DSNCs with a 2 nm interfacial HfO$_2$ thickness ($t_{\text{inter}}$ = 2 nm). The gate voltage was double swept from positive to negative voltage. The DSNCs with a 2 nm interfacial HfO$_2$ thickness proved to have the same number of Ag NCs. In the negative program, the shift of flatband voltage for various ranges of the gate voltage in DSNCs with a 2 nm interfacial HfO$_2$ thickness ($t_{\text{inter}}$ = 2 nm) showed large counterclockwise C-V hysteresis, which clearly reveals the charge storage effect. The initial hysteresis in the first control group was 300 mV, as shown in the inset of Fig. 1. The negligible hysteresis indicates that the C-V hysteresis in DSNCs ($t_{\text{inter}}$ = 2 nm) stems not from defects or gate dielectrics but solely from the Ag NCs.

Figure 3 shows the result of flatband voltage shifts ($\Delta V_{\text{fb}}$) for various program voltages of the SSNCs and two types of DSNCs ($t_{\text{inter}}$ = 2 nm and $t_{\text{inter}}$ = 6 nm) in order to examine program efficiency at a fixed program time ($\tau_p$ = 1 s). The thicker DSNCs ($t_{\text{inter}}$ = 6 nm) show less $\Delta V_{\text{fb}}$ but a steeper slope than the thinner DSNCs ($t_{\text{inter}}$ = 2 nm). The charges injected into the upper NCs layer came mainly from the trapped charges in the lower NCs layer via the interfacial HfO$_2$. The tunneling mechanism depends on not only the thickness of the interfacial HfO$_2$, which affects the charge retention characteristic in the upper NCs layer, but also electric field across the interfacial HfO$_2$. The dominant charge injection mechanisms are the direct tunneling or trap-assisted tunneling for both cases; $t_{\text{inter}}$ = 2 nm and $t_{\text{inter}}$ = 6 nm even at the low electric field caused by the thick control oxide of 23 nm. Thus, the thicker DSNCs ($t_{\text{inter}}$ = 6 nm) need a larger program voltage than the thinner DSNCs ($t_{\text{inter}}$ = 2 nm) to get the same amount of $\Delta V_{\text{fb}}$ because of the lower tunneling possibility of charges in $t_{\text{inter}}$ = 6 nm. But, as the gate voltage increases, $\Delta V_{\text{fb}}$ becomes saturated and the discrepancy of $\Delta V_{\text{fb}}$ between both cases diminishes. The reason of the diminishment is that the electron injection current from the substrate to the storage nods tends to be the same as the emission current from the storage nods to the gate. Furthermore, both types of DSNCs ($t_{\text{inter}}$ = 2 nm and $t_{\text{inter}}$ = 6 nm) have the same number of Ag NCs. In the negative program
The probability of electrons tunneling through a rectangular barrier was simply modeled. The transmission coefficient via the dielectric barrier exponentially decreases as the barrier width (dielectric thickness) and the barrier height increase. The barriers that prevented the stored charges from lateral tunneling were made of 3.3 nm of control oxide in the NC-to-NC space of the SSNCs and 2 nm of interfacial dielectric HfO2 in the DSNCs. The barrier width of the control oxide was 3.3 nm and the barrier height of the control oxide was 4.1 eV in the Ag SSNCs, whereas the barrier width of the interfacial HfO2 was 2 nm and the barrier height of the interfacial HfO2 was 2.5 eV in the thinner Ag DSNCs ($t_{\text{inter}}=2$ nm). The calculated transmission coefficient of thinner DSNCs ($t_{\text{inter}}=2$ nm) is 10^9 times larger than that of the SSNCs. The ratio of the measured retention time of the SSNCs to the extrapolated retention time of the DSNCs is roughly 10^9 when $\Delta V_\text{fb}$ is zero in Fig. 4(a).

In summary, the thermal decomposition method was used to synthesize uniform, well-ordered Ag NCS forming SSNCs and DSNCs. The nonvolatile memory characteristics were achieved and analyzed for the thickness modulation effect of the interfacial HfO2 by using MOS structures with SSNCs and with two types of DSNCs ($t_{\text{inter}}=2$ nm and $t_{\text{inter}}=6$ nm). The thicker DSNCs ($t_{\text{inter}}=6$ nm) showed the best retention characteristic for all samples. When the interfacial layer is thinner than 3 nm, the retention characteristic conspicuously worsens due to the sawtoothed lateral tunneling of the stored charges. The trade-off was identified between the P/E efficiency and the charge retention for different interfacial HfO2 thicknesses in the DSNCs.

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FIG. 4. (a) The retention time characteristics for the SSNCs ($d_{\text{avg}}=4$ nm, $t_{\text{tunnel}}=4.5$ nm), the thinner DSNCs ($d_{\text{avg}}=4$ nm, $t_{\text{tunnel}}=4.5$ nm, $t_{\text{inter}}=2$ nm), and the thicker DSNCs ($d_{\text{avg}}=4$ nm, $t_{\text{tunnel}}=4.5$ nm, $t_{\text{inter}}=6$ nm) at room temperatures and with P/E voltages of +9 V/−9 V, +9 V/−9 V, and +11 V/−13 V, respectively. Schematic of the charges’ leakage paths are illustrated for (b) the SSNCs and (c) the thinner DSNCs ($d_{\text{avg}}=4$ nm, $t_{\text{tunnel}}=4.5$ nm, $t_{\text{inter}}=2$ nm). The charge retention of the thinner DSNCs ($d_{\text{avg}}=4$ nm, $t_{\text{tunnel}}=4.5$ nm, $t_{\text{inter}}=2$ nm) is worse than that of the SSNCs ($d_{\text{avg}}=4$ nm, $t_{\text{tunnel}}=4.5$ nm) due to the lateral sawtoothed tunneling of the stored charges.

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