High Temperature Characteristics of SOI and Body-Tied FinFETs

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INTRODUCTION

A FinFET offers the superior scalability of CMOS with a conventional process [1]. Due to the high power consumption resulting from scaled-down devices, the temperature characteristics of the FinFET have become a major concern. For the first time, the temperature dependency of fully depleted SOI and body-tied FinFETs is investigated with consideration of fin width scaling.

EXPERIMENT

The fabrication details for the SOI and body-tied FinFETs used in this study have been reported elsewhere [2][3]. The device schematics of both FinFETs are shown in Fig. 1. For a fair comparison between the two structures, all currents are normalized by the channel width. The typical device dimensions and measurement conditions are summarized in Table 1. All devices used for characterization are NMOS.

RESULTS

The temperature dependency of the drain current (I_D) versus gate voltage (V_G) is shown in Fig. 2 and Fig. 3 for the body-tied FinFETs and the SOI FinFETs, respectively. The off-state current (I_OFF) for both structures was increased by carrier diffusion as the substrate temperature (T) increases. However, the on-state current (I_ON) was reduced by carrier mobility (μ) degradation as T increases in the body-tied FinFETs. There are two competing factors that govern I_ON at elevated T: threshold voltage (V_T) drop and μ degradation due to I_OFF ∝ μ(V_G−V_T)². In the SOI FinFETs, μ is degraded and V_T rapidly drops off as T rises. Thus, I_ON at high T becomes larger than at room T, as shown in Fig. 3. The following shows a quantitative analysis of the temperature dependence of the device parameters.

The subthreshold slope (SS) degradation with elevated T causes a power consumption problem due to the off-state leakage current. As shown in Fig. 4, SS was linearly degraded as T increased in the body-tied FinFETs, whereas SS rapidly increased from T=125°C in the SOI FinFETs. This non-linear behavior of SS originates from the increase of effective body capacitance [4]. V_T variation is an important concern for stable circuit operation with a wide range of T. In order to investigate the temperature immunity for V_T, the temperature coefficient of V_T (ΔV_T/ΔT) was extracted from the measured data, as shown in Fig. 5. ΔV_T/ΔT was -1.5mV/K and -1.2mV/K for 18nm and 26nm fin width in the SOI FinFETs; thus, the high temperature operation stability is enhanced as the fin width increases. ΔV_T/ΔT (-0.5mV/K) of the body-tied FinFETs was lower than that of the SOI FinFETs and independent of the fin width, which is attractive for circuit operation in a wide range of T. In Fig. 6, I_ON near the sub-threshold (V_G=V_T) is lower in the SOI than in the body-tied FinFETs at room T. This is due to the low fraction of diffusion current arising from the small junction area. However, as T increases, I_OFF/V_T of the SOI FinFETs crosses over that of the body-tied FinFETs. This trend is attributed to the rapid increase of the SS of SOI FinFETs as T is elevated, as shown in Fig. 4. In Fig. 7, I_ON monotonously decreases due to the mobility degradation by phonon-scattering in the body-tied FinFETs. However, in the SOI FinFETs, I_ON increases as T increases beyond 75°C. The zero-temperature-coefficient point (Fig. 8) at V_G=1V, which is a result of competition between the μ degradation and V_T drop, is higher than V_G=0.6V for the SOI FinFETs. This is consistent with the observation of higher ΔV_T/ΔT of SOI FinFETs relative to that of body-tied FinFETs. As a result, below 1V operational voltage, the V_T drop leads to an increment of I_ON, which compensates I_ON by μ degradation in the SOI FinFETs.

SUMMARY

The body-tied FinFET displayed better immunity to temperature variation than the SOI FinFET in terms of I-V characteristics. For body-tied FinFETs, the temperature dependency of the device parameters is insensitive to the fin width. For SOI FinFETs, however, a wider fin is more favorable for use in a wide range of temperatures. In the case of operational voltage below 1V, the on-current of SOI FinFETs increases in spite of the mobility degradation at high temperature operation.

REFERENCES


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**Fig. 1** Schematic of the FinFET (a), Cross-section view of a SOI FinFET (b) and a body-tied FinFET (c).

**Fig. 2** $I_D$ versus $V_G$ at various temperatures for the body-tied FinFET. $I_{off}$ reduces and $I_{ON}$ increases as $T$ increases.

**Fig. 3** $I_D$ at high temperature becomes larger than at room temperature due to a rapid $V_T$ drop off.

**Fig. 4** Subthreshold slope (SS) versus $T$. SS linearly increases as $T$ increases in the body-tied FinFETs whereas SS rapidly jumps up from $T=125^\circ C$ in the SOI FinFETs.

**Fig. 5** $\Delta V_T$ versus $T$. $\Delta V_T/\Delta T$ is $-1.5$ mV/K and $-1.2$ mV/K for 18nm and 26nm fin width in the SOI FinFETs and $-0.5$ mV/K in the body-tied FinFETs.

**Fig. 6** $I_D@V_T$ versus $T$. As temperature increases, $I_D@V_T$ at the SOI FinFETs increases, and crosses over the body-tied FinFETs. Thermally generated diffusion current is dominant despite its small junction area arising from its low thermal conductivity.

**Fig. 7** $I_{ON}$ versus $T$. $I_{ON}$ is decreasing due to mobility degradation. However, $I_{ON}$ increases as $T$ increases because of $V_T$ drop beyond $75^\circ C$ in the SOI FinFETs.

**Fig. 8** $I_D$ versus $V_G$. In SOI FinFETs, at 1V operational voltage, $V_T$ drop leads $I_{ON}$ increment, which compensates $I_{OFF}$ by the mobility degradation.

**Table 1** Device dimensions and measurement conditions.