Sublithographic nanofabrication technology for nanocatalysts and DNA chips

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We describe parallel processes for nanometer pattern generation on a wafer scale with resolution comparable to the best electron beam lithography. Sub-10 nm linewidth is defined by a sacrificial ultrathin film deposited by low pressure chemical vapor deposition (LPCVD), in a process similar to formation of gate sidewall spacers in CMOS processing. We further demonstrate a method called iterative spacer lithography (ISL), in which the process is repeated multiple times with alternating materials in order to multiply the pattern density. Silicon structures with sub-10 nm width fabricated by this process were used as a mold in nanoimprint lithography and lift-off patterning of sub-30 nm platinum nanowires for use in experiments on chemical catalysis. We also demonstrate a similar process called reversed spacer lithography (RSL) to form sub-10 nm fluid channels in poly-Si. This nanogap fluid channel device was used for label-free detection of DNA hybridization based on electrical sensing of dielectric changes in the gap. © 2003 American Vacuum Society. [DOI: 10.1116/1.1627805]

I. INTRODUCTION

Sub-50 nm features have commonly been fabricated by electron beam lithography, which is an expensive technique due to its low throughput. In this paper, we describe parallel processes for nanometer pattern generation on a wafer scale with resolution comparable to the best electron beam lithography. The technique is based on the conformal deposition of a thin-film material by low pressure chemical vapor deposition (LPCVD) over a previously patterned step in a sacrificial material. By depositing a material that has a different etching property than the sacrificial layer and directionally etching the material on the top of the step, the sacrificial layer can then be removed selectively, leaving only the material deposited on the sidewall, as shown in Fig. 1(a). This process is similar to the formation of gate sidewall spacers in CMOS processing and we refer to it as "spacer lithography." The feature size thus generated is determined by the thickness of the deposited material, not by a conventional lithography process.\(^1,2\) Since the thickness of the deposited film can be controlled to 10 nm or less with high precision, this method is capable of generating sub-10 nm patterns as shown in Figs. 1(b) and 1(c). In addition, it also provides a doubling of the pattern density for a given lithography pitch because two symmetrical spacers are generated for each sacrificial line in the dummy layer.\(^2\) Starting with a 0.6 μm line and 1.2 μm space pattern formed by optical lithography and then iterating this process and alternating the sidewall and sacrificial materials, dense nanowires with sub-100 nm spacing can be fabricated on a wafer scale as shown in Fig. 2. This method can be used to pattern silicon fins for double-gate MOSFETs (FinFETs).\(^3,4\)

The nanopattern generated by spacer lithography can easily cover an entire wafer and can be used as a mold for nanoimprint lithography. The large nanopatterned area permits unique studies of chemical catalysis. We formed arrays of 30 nm Pt nanowires for this purpose. A 10 nm silicon nanoimprint mold was first fabricated using spacer lithography. Then, using nanoimprint patterning in PMMA and lift-off processing, 30 nm Pt nanowire arrays were fabricated, as shown in Fig. 3. Catalytic properties of these structures are currently under investigation.

A complementary version of this process is reversed spacer lithography (RSL), which is used to fabricate gaplike patterns. In this case, the thin spacers are sacrificial layers and the supporters are structure layers. This type of structure can be used to fabricate a nanogap device that is used for detection of DNA hybridization. Various techniques

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such as fluorescence, electrochemical, enzymatic, and magnetic have been developed to detect hybridization of DNA. Unfortunately, these methods require labeling steps, which are unwieldy and time-consuming procedures. Label free hybridization detection technology remains a highly desirable goal. In this work, a novel approach for label free detection of DNA hybridization by utilizing nano-gap electrodes is reported with dielectric spectroscopy. For enhancement of detection sensitivity, the nanogap is required to eliminate parasitic capacitance coming from induced counterions.

II. FABRICATION AND CHARACTERIZATION

The spacer lithography process reported here extends upon the work previously demonstrated for fabricating nanoscale fins for the double-gate FinFET. A 100 nm thickness of poly-Si is deposited on the hard mask oxide by LPCVD. This poly-Si serves as a sacrificial support to hold the sidewall spacers. It is patterned by an i-line lithography and plasma reactive ion etching (RIE). A 40 nm thickness of low temperature oxide (LTO) is deposited by LPCVD and etched back. The poly-Si is removed by HBr based plasma etch, which provides high etch selectivity of poly-Si to oxide (200:1). Thereafter, sub-20 nm sidewall oxide spacers are left and they can serve as an etching mask to pattern the underlying crystal silicon. These relatively tall spacers are transferred to the hard mask oxide by CF$_3$ plasma. Continuously, the crystal silicon is anisotropically etched by Cl$_2$ based plasma. After thermal oxidation and HF wet etching, the sub-20 nm crystal silicon pattern is reduced down to 7 nm as shown in Fig. 1(c).

To further increase the pattern density, iterative spacer lithography (ISL) is demonstrated as shown in Fig. 2. A 150 nm thick silicon nitride layer is deposited by LPCVD. This nitride has high wet etching selectivity to poly-Si in KOH and oxide in HF. Then, a 1 $\mu$m thickness of heavily n-type in situ doped poly-Si is deposited to become supporters of the sidewall oxide and patterned anisotropically using an i-line photolithography. A 450 nm LTO film is deposited and etched back such that LTO on the top of the poly-Si and on the substrate nitride are eliminated. The remaining sacrificial poly-Si is removed by wet etching in KOH, and tall oxide spacers with half the original lithography period are left. For this step, the oxide spacers are structure layers while the poly-Si patterns are sacrificial layers. In the second iteration, a 300 nm thickness of the second poly-Si is deposited and etched back. Now the oxide spacers are sacrificial layers while the second poly-Si spacers are structure layers. The oxide spacers are wet etched away by diluted HF, which result in doubling the number of lines again. In the third and final iteration, a 190 nm thick layer of the second CVD oxide is deposited and etched back. After elimination of the second poly-Si by wet etching in KOH, the line density is doubled again as shown in Fig. 2(a). Figure 2(b) shows the tilted view of SEM photographs after the first poly-Si patterning, the first oxide spacer formation, the second poly-Si spacer formation, and the third oxide spacer formation, respectively.
Some potential applications of ISL are to make dense silicon fins to increase the drive current resulting in improvement of speed in double-gate FinFET CMOS microelectronics, and high density memory devices with organic material for nanoscale computing.

The Si nanowire structures fabricated by ISL can be used as a mold for producing high surface area devices by nanoimprint lithography. The process flow for nanoimprint patterning is shown in Fig. 3(a). The residual PMMA after imprint and mold separation is eliminated by O₂ RIE. Due to an isotropic contribution to the PMMA etching, the gap width in the PMMA pattern is increased to 30 nm. Then, platinum (Pt) is evaporated, and lifted off by acetone, assisted with ultrasonication as shown in Fig. 3(b). Thus, 10 nm silicon mold structures are transformed to 30 nm Pt wires as shown in Fig. 3(c). Catalytic properties of these structures are currently under investigation.

Combining sublithographic nanofabrication and nanoimprint technology can enable the patterning of different types of nanoscale materials, which can be used for chemical sensors or biosensors because the surface charge is comparable to the bulk charge in such narrow wires.

The RSL process is used to make nanogaps. In this process, spacers and supporters are switched, i.e., spacers are sacrificial layers and supporters are structure layers. A 400 nm thick layer of silicon nitride is deposited by LPCVD to isolate two electrodes from the crystalline silicon substrate. A 1 μm layer of n-type heavily in situ doped poly-Si is deposited by LPCVD to make the grounded electrodes (denoted as “II” in Fig. 4) of the vertical capacitor. To activate dopants in the in situ doped poly-Si, they are annealed at 900 °C for 1 min with rapid thermal annealing. After CMP, the top poly-Si and the LTO hard mask were completely etched-back and planarized as shown in Fig. 4(a). Next, the sacrificial sidewall LTO is removed by wet etching 10:1 H₂O/HF. During this release process, the nitride insulator underneath the poly-Si (I) and (II) were not etched thus avoiding any isotropic undercut profiles. Figure 4(b) shows cross-sectional scanning electron microscopy (SEM) photographs of a 50 nm gap along the z–z’ direction in Fig. 4(a). More recently, we have fabricated sub-10 nm nanogap capacitors using a thickness of 10 nm high temperature oxide (HTO). These can also be used to confine nanobeads or nanorods, or they can be utilized to manipulate single molecules for investigation of their electrical properties.

Nanogap capacitor arrays provide label free DNA hybridization detection as shown in Fig. 5. For convenience, a

**Fig. 3.** Schematic process flow of nanoimprint (a), lift-off as well as Pt evaporation (b), and SEM photograph of fabricated Pt nanowire arrays (c) for catalysis studies.

**Fig. 4.** Process flow of nanogaps (a) and cross-sectional SEM photographs (b). The gap width is determined by the deposited oxide film thickness.
single capacitor with 50 nm gap patterned by LTO is used for DNA hybridization detection. A dc and small signal ac bias (25 mV) is applied to the first electrodes [poly-Si (I)] and the second electrodes [poly-Si (II)] are grounded. The meandering structures of the poly Si (I) maximize the capacitive area while the total capacitor size in top view is to be minimized.

3-aminopropyl triethoxysilane is used as a self-assembled monolayer (SAM) to enhance the efficiency of immobilization of DNAs. Next, T_{35} (35-mer-oligonucleotides) are coated on top of the SAM for immobilization so that the 5' end of single-stranded DNA (ssDNA) is linked to the amine group on the SAM. A_{35} and G_{35} are used to check hybridization. For proof of concept of DNA hybridization detection, a T–A conjugative base pairs are made. However, there is no significant difference of the measured capacitance before and after hybridization in the case of nonconjugated DNA strands as shown in Fig. 5(b). Similar behavior is also observed in G_{15}–C_{15} pairs. The reason for the capacitance difference between ssDNA and dsDNA is related to the geometrical structures and induced counter ion profile. Theoretical modeling of this process will be reported in the near future.

III. SUMMARY

Sublithographic nanowires and nanogaps were fabricated by spacer lithography. Iterative spacer lithography (ISL) was developed and demonstrated as a technique to multiply the pattern density, enabling fabrication of dense, sub-100 nm patterns starting with low-resolution optical lithography. We showed a few example applications of these techniques. Pt nanowires for use in catalysis experiments were formed using a silicon structure fabricated by spacer lithography as a nanoimprint mold, followed by Pt evaporation, and lift-off. Nanogap vertical capacitors were fabricated by reversed spacer lithography (RSL) and used for the detection of DNA hybridization without labeling. DNA hybridization was detected by capacitance measurements, and the capacitance was found to increase as input frequency decreases when hybridization occurs. Due to the full compatibility with silicon microfabrication technology, DNA chips without any requirement of a labeling process are thus feasible which can reduce the cost and dramatically speed up assays of DNA hybridization.

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