Sub-Lithographic Patterning Technology for Nanowire Model Catalysts and DNA Label-Free Hybridization Detection

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ABSTRACT

Sub-lithographic nanowires and nanogaps were fabricated by spacer lithography (size reduction technology), which is a parallel processes for nanometer pattern generation on a wafer scale with resolution comparable to the best electron beam lithography. Sub-10nm line width is defined by using a sacrificial ultra-thin film deposited by low pressure chemical vapor deposition (LPCVD), in a process similar to formation of gate sidewall spacers in CMOS processing. Furthermore, a novel method called iterative spacer lithography (ISL) is demonstrated by alternating materials and repeating the spacer lithography multiple times in order to multiply the pattern density. Silicon structures with sub-10nm width fabricated by this process were used as a mold in nanoimprint lithography and lift-off patterning of sub-30nm platinum nanowires for use as model catalyst systems. A similar process called reversed spacer lithography (RSL) is demonstrated to form sub-10nm nanogap device and fluid channels in poly-Si. This nanogap device provides a label-free tool for DNA hybridization detection based on measuring capacitance changes in the gap.

Keywords: Sub-lithographic technology, nanofabrication, iterative spacer lithography, reversed spacer lithography, nanowire, nanogap, label free DNA hybridization detection, platinum catalysts

1. INTRODUCTION

Defining sub-50nm features is still a challenging task with optical lithography. Electron beam lithography has commonly been used to define such small features. However, it is an expensive technique due to its low throughput. In this paper, parallel processes for nanometer pattern generation on a wafer scale are described. Its resolution is comparable to the best electron beam lithography. The technique is based on the conformal deposition of a thin-film material by low pressure chemical vapor deposition (LPCVD) over a previously patterned step in a sacrificial (dummy) material. By depositing a material that has a different etching property than the sacrificial layer and directionally etching the material on the top of the step, the sacrificial layer can then be removed selectively, leaving only the material deposited on the sidewall, as shown in Fig. 1 (b). This process is similar to the formation of gate sidewall spacers in CMOS processing, and we refer to it as “spacer lithography (size reduction technology)”. The feature size thus generated is determined by the thickness of the deposited material, not by a conventional lithography process. Since the thickness of the deposited film can be controlled to 10 nm or less with high precision, this method is capable of generating sub-10 nm patterns as shown in Fig. 1 (b). In addition, it also provides a doubling of the pattern density for a given lithography pitch, because two symmetrical spacers are generated for each sacrificial line in the dummy layer.
Figure 1. Schematic view and SEM photographs of nanostructures by spacer lithography. Minimum sized features are defined by the deposited film thickness in the spacer lithography while they are defined by the resist width in the conventional lithography. In a given pitch, pattern density is doubled in the spacer lithography.

Starting with a 0.6μm line and 1.2μm space pattern formed by optical (i-line) lithography and then iterating this process and alternating the sidewall and sacrificial materials, dense nanowires with sub-100 nm spacing can be fabricated on a wafer scale as shown in Fig. 2. This process provides a density increase as well as size reduction. It can be used to pattern silicon fins for double-gate MOSFETs (FinFETs)\textsuperscript{1,2}.

Figure 2. Schematic view of iterative spacer lithography (ISL).
The nanopattern generated by spacer lithography\textsuperscript{2,14} can easily cover an entire 4" wafer and can be used as a mold for nanoimprint lithography\textsuperscript{3}. The dense nanopatterned area permits unique studies of chemical catalysis\textsuperscript{15}. We formed arrays of 30 nm Pt nanowires for this purpose. A 10nm silicon nanoimprint mold was first fabricated using spacer lithography (size reduction technology). Then, using nanoimprint patterning in PMMA, metal deposition with electron beam evaporation, and lift-off processing, 30 nm Pt nanowire arrays were fabricated. Catalytic properties of these structures are currently under investigation.

A complementary version of this process is reversed spacer lithography (RSL), which is used to fabricate gap-like patterns. In this case, the thin spacers are sacrificial layers and the supporters are structure layers. This type of structure can be used to fabricate a nanogap device that is used for detection of DNA hybridization. Fluorescence\textsuperscript{4,5}, electrochemical\textsuperscript{6,7}, enzymatic\textsuperscript{8,9}, and magnetic\textsuperscript{10} techniques have been developed to detect hybridization of DNA. These methods require labeling steps, which are unwieldy and time-consuming procedures. Label-free hybridization detection technology remains a highly desirable goal. In this work, a novel approach for label-free detection of DNA hybridization by utilizing nanogap electrodes for dielectric spectroscopy is reported. For enhancement of detection sensitivity, the nanogap is required to eliminate parasitic capacitance coming from induced counter ions.

2. DEVICE FABRICATION AND CHARACTERIZATION

2.1 Silicon nanowires

The spacer lithography process reported here extends upon the work previously demonstrated for fabricating nanoscale fins for the double-gate FinFET\textsuperscript{1,2}. A 50nm thick hard mask oxide is thermally grown on a (100) silicon wafer. A 100nm thickness of poly-Si is deposited on the hard mask oxide by LPCVD. This poly-Si serves as a sacrificial support for the sidewall spacers. It is patterned by i-line ($\lambda$=365nm) lithography and plasma reactive ion etching (RIE). A 40nm thickness of low temperature oxide (LTO) is deposited by LPCVD and etched back. The poly-Si is removed by an HBr-based plasma etch, which provides high etch selectivity of poly-Si to oxide (200:1). Thereafter, sub-20nm sidewall oxide spacers are left and they can serve as an etching mask to pattern the underlying crystalline silicon. These relatively tall spacers are transferred to the hard mask oxide by CF$_4$ plasma etching. The crystalline silicon is then anisotropically etched by a Cl$_2$-based plasma. After thermal oxidation and HF wet etching, the sub-20nm crystalline silicon pattern is reduced down to 7nm as shown in Fig. 1 (c).

This structure is used as a mold in nanoimprint lithography to make sub-30nm platinum nanowires for use as model catalyst systems. Similarly, sub-20nm crystalline silicon nanowires are made on a SOI (Silicon-on-insulator) wafer. It is heavily doped with phosphorus ion implantation and activated at the high temperatures. Then, aluminum is evaporated on the patterned resist and lifted-off for probing and low interconnection resistance as shown in Fig. 3. These crystalline Si nanowires can be used for chemical sensors\textsuperscript{11}.

![Figure 3. Schematic view and sub-20nm crystalline Si nanowires with Al pads for chemical sensors. The top view of Si sensors is close-up view of a circle in the inset.](image-url)
To further increase the pattern density, iterative spacer lithography (ISL or multiple size reduction technology) is demonstrated as shown in Fig. 2 and Fig. 4. A 150nm thick silicon nitride layer is deposited by LPCVD. This nitride has high wet etching selectivity to poly-Si in KOH and oxide in HF. Then, a 1µm thickness of heavily n-type in-situ doped poly-Si is deposited and patterned anisotropically using i-line photolithography. A 450nm LTO film is deposited and etched back such that LTO on the top of the poly-Si and on the substrate nitride are eliminated. The remaining sacrificial poly-Si is removed by wet etching in KOH, and tall oxide spacers with half the original lithography period are left. For this step, the oxide spacers are structure layers while the poly-Si patterns are sacrificial layers. In the second iteration, a 300nm thickness of the second poly-Si is deposited and etched back. Now the oxide spacers are sacrificial layers while the second poly-Si spacers are structure layers. The oxide spacers are wet etched away by diluted HF, which results in doubling the number of lines again. In the third and final iteration, a 190nm thick layer of the second CVD oxide is deposited and etched back. After elimination of the second poly-Si by wet etching in KOH, the line density is doubled again as shown in Fig. 2. Fig. 4 shows the top view of SEM photographs after the first poly-Si patterning, the first oxide spacer formation, the second poly-Si spacer formation, and the third oxide spacer formation, respectively. Some potential applications of ISL are to make dense silicon fins to increase the drive current resulting in improvement of speed in double-gate FinFET CMOS microelectronics\textsuperscript{12}, and high density memory devices\textsuperscript{13} with organic material for nanoscale computing.

![Figure 4. Top view SEM photographs of high density nanowires by iterative spacer lithography (ISL) in Fig. 2. 8 (=2\(^5\)) lines were generated after 3 times spacer lithography. Line width was 70nm and space was 80nm in (VI). The photographs denoted by Roman number are corresponding to the schematics in Fig. 2.](image)

### 2.2 Platinum nanowires

The Si nanowire structures fabricated by ISL (multiple size reduction technology) can be used as a mold for producing high surface area devices by nanoimprint lithography. Combining sub-lithographic nanofabrication and nanoimprint technology can enable the patterning of different types of nanoscale
materials, which can be used for chemical sensors or bio-sensors because the surface charge is comparable
to the bulk charge in such narrow wires. The techniques of spacer lithography (size reduction technology) and
nanoimprint lithography employed to produce the Pt nanowire sample overcome the problems of electron
beam lithography in that structures are reproducibly fabricated that are sub-10 nm, the process is not serial,
and the amount of surface area that can be patterned is of the order of cm$^2$ instead of mm$^2$. The process has
been demonstrated to yield well-defined structures that are uniform in size and interstructure distance as well
as choice of metal and oxide support combinations$^{14}$.

Nanoimprint lithography is used to deform the physical shape of the resist by embossing with a mold.
This has many benefits to make nanostructures such as patterns of noble metal and bio-molecules. The
process flow for nanoimprint patterning is shown in Fig. 5 (a). The residual PMMA after imprint and mold
separation is eliminated by O$_2$ RIE. Due to an isotropic contribution to the PMMA etching, the gap width in
the PMMA pattern is increased to 30nm. Then, platinum (Pt) is evaporated, and lifted off by acetone, assisted
with ultrasonication as shown in Fig. 5. Thus, 10nm silicon mold structures are transformed to 30nm Pt wires
as shown in Fig. 5 (c). Structure-sensitive reactions, such as hydrocarbon reforming reactions over platinum,
will be the focus of future studies. This will enable us to gain insight into those molecular ingredients that
make industrial catalysts both active and selective, such as the size dependence and therefore the metal
surface structure and the number of oxide-metal interface sites.

![Nanoimprint schematic](image)

(a) After nanoimprint and removal of residual PMMA by O$_2$ plasma

![Pt evaporation](image)

(b) Pt evaporation and lift-off

![SEM photograph](image)

(c) SEM photograph of 30nm width of Pt nanowires

![Activation energy](image)

(d) Measured activation energy for ethylene hydrogenation to ethane

Figure 5. Process schematics for Pt nanowire arrays with nanoimprint and lift-off as well as Pt evaporation, top view SEM photograph of 30nm width of Pt nanowires, and turnover frequency (TOF) versus temperature.
A platinum nanowire model catalyst sample on silica was placed into an ultrahigh vacuum surface science chamber coupled with a high-pressure reaction cell for catalysis reaction studies. The catalyst sample had 10% total coverage of Pt. The structure-insensitive ethylene hydrogenation reaction was utilized as a test catalytic reaction so that results from other model catalysts systems, such as Pt(111) single crystal and Pt nanoparticles supported on Al$_2$O$_3$, can be compared; the reaction can also be used to effectively determine the active metal surface area$^{15}$. The effects of support (Al$_2$O$_3$ and SiO$_2$) and CO poisoning will be analyzed in a forthcoming paper.

The effectiveness of a catalyst for a reaction is measured in terms of a turnover frequency, which is the number of molecules reacting per active site per second. An Arrhenius plot of the natural log of turnover frequency versus inverse temperature yields the barrier or activation energy that must be overcome for a reaction to proceed. As can be seen in Fig. 5 (d), the measured activation energy for ethylene hydrogenation to ethane was 13.0 ± 0.3 kcal/mol. This compares well to other model catalyst systems$^{16}$. However, the amount of platinum sites, the choice of support, and the number of oxide-metal interface sites, all of which affect a reaction’s turnover, were not constant from one model catalyst system to the next. Therefore, further experiments are conducted to normalize these results.

### 2.3 Nanogap devices for label free DNA hybridization detection

The RSL process is used to make nanogaps. In this process, spacers and supporters are switched, i.e., spacers are sacrificial layers and supporters are structure layers. A 400 nm thick layer of silicon nitride is deposited by low pressure chemical vapor deposition (LPCVD) to isolate two electrodes from the crystalline silicon substrate. A 1 \( \mu \)m layer of n-type heavily in-situ doped poly-Si is deposited to make the first electrodes (denoted as ‘I’ in Fig. 6) of the vertical capacitor by LPCVD. Next, a 300 nm thick layer of LPCVD low temperature oxide (LTO) is deposited. The LTO layer serves as a hard mask to protect the electrode (I) during subsequent chemical-mechanical polishing (CMP) because the polishing rate is faster at the protruded patterns than at the flat patterns. The electrode (I) is then defined using i-line lithography and anisotropic etching. Next, a 100nm layer of sacrificial LTO is deposited by LPCVD. This process is the critical step of RSL, since it determines the nanogaps. The sacrificial LTO on the top of the poly-Si is then removed by etch-back, which does not require any masks. Thus, sidewall LTO is left along the electrode (I) as shown in Fig. 6 (a). A 1\( \mu \)m layer of n-type heavily in-situ doped poly-Si is deposited by LPCVD to make the grounded electrodes (denoted as “II” in Fig. 6) of the vertical capacitor. To activate dopants in the in-situ doped poly-Si, they are annealed at 900 °C for 1 min with rapid thermal annealing. After CMP, the top poly-Si and the LTO hard mask is completely etched-back and planarized as shown in Fig 6 (a). Next, the sacrificial sidewall LTO is removed by wet etching in (10:1) H$_2$O/HF. During this release process, the nitride insulator underneath the poly-Si (I) and (II) is not etched, thus avoiding any isotropic undercut profiles. Fig. 6 (b) shows cross-sectional scanning electron microscopy (SEM) photographs of a 100 nm gap filled with DNA after hybridization and dry-up along the z-z' direction in Fig. 6 (a). More recently, we have fabricated sub-10 nm nanogap capacitors using a 10 nm thickness of high temperature oxide (HTO) as shown in Fig 7 (b). These can also be used to confine nanobeads or nanorods, or they can be utilized to manipulate single molecules for investigation of their electrical properties.
Nanogap capacitor arrays provide label-free DNA hybridization detection as shown in Fig. 6. For convenience, a single capacitor with a 100nm gap patterned by LTO is used for DNA hybridization detection. A DC and small signal AC bias (25 mV) is applied to the first electrodes (poly-Si (I)), and the second electrodes (poly-Si (II)) are grounded. The meandering structures of the poly-Si (I) maximize the capacitive area, while the total capacitor size in the top view is to be minimized.

3-aminopropyl triethoxysilane is used as a self-assembled monolayer (SAM) to enhance the efficiency of immobilization of DNAs. Next, G$_{35}$ (35-mer-oligonucleotides) are coated on top of the SAM for immobilization so that the 5’ end of single-stranded DNA (ssDNA) is linked to the amine group on the SAM. C$_{35}$ and T$_{35}$ are used to check hybridization detection. For proof of concept of DNA hybridization detection by using capacitance measurement, a simple G-C combination is selected. All oligonucleotides used in this experiment are produced by Alpha DNA, Inc. The inset of Fig. 7 (a) shows a schematic illustration of ssDNA, which is randomly tangled, and double-stranded DNA (dsDNA), which is relatively stretched out. Additional details of the sample preparation are reported elsewhere. The capacitance with ssDNA and dsDNA is measured using an HP4284A LCR meter before and after hybridization. Fig. 7 (a) shows that, as the input frequency decreases, the capacitance increases more rapidly after hybridization than before.
hybridization. However, there is no significant difference of the measured capacitance before and after hybridization in the case of non-conjugated DNA strands. Similar behavior is also observed in G-T₃₅ pairs. The reason for the capacitance difference between ssDNA and dsDNA is related to the geometrical structures and induced counter ion profile. Theoretical modeling of this process will be reported in the near future.

Figure 7. Capacitance increases as the frequency decreases in the conjugated base pairs (G-C) and there is no significant difference of capacitance in the non-conjugated base pairs (G-T).

2.4 Nanofluidic channels

Similarly, the RSL process is used to make nanofluidic channels. A 100nm thick layer of crystalline silicon is anisotropically etched. This etching target will control the height of fluidic channels. Then, 10nm of high temperature oxide (HTO) is conformally deposited and etched-back. This HTO film thickness determines the width of the fluidic channels. A 140nm thick layer of undoped poly-Si is deposited to encapsulate the channels. After patterning the poly-Si, the spacer HTO is removed by HF wet etching as shown in Fig. 8. This sub-10nm fluidic channel can be used to mimic ion channels in a cell membrane.

Figure 8. Sub-10nm vertical nanofluidic channels fabricated by the reversed spacer lithography (RSL).
3. SUMMARY

Sub-lithographic nanowires and nanogaps were demonstrated with spacer lithography (size reduction technology). Iterative spacer lithography (ISL) or multiple size reduction technology was developed and demonstrated as a technique to multiply the pattern density, enabling fabrication of dense, sub-100 nm patterns starting with low-resolution optical lithography. Pt nanowires for use in catalysis experiments were fabricated using a silicon structure fabricated by spacer lithography (size reduction technology) and nanoimprint lithography, followed by electron beam evaporation of Pt, and lift-off. The effectiveness of the Pt nanowire catalyst for a reaction was comparable to other Pt model catalysts. Nanogap vertical capacitors were fabricated by reversed spacer lithography (RSL) and used for the detection of DNA hybridization without labeling. DNA hybridization was detected by capacitance measurements, and the capacitance was found to increase as input frequency decreases when hybridization occurs.

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REFERENCES


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