Spacer FinFET: nanoscale double-gate CMOS technology for the terabit era

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Abstract

A spacer lithography technology using a sacrificial layer and a chemical vapor deposition (CVD) spacer layer has been developed, and is demonstrated to achieve sub-40 nm structures with conventional dry etching. The minimum-sized features are finished not by photolithography but by the CVD film thickness. Therefore the spacer lithography technology yields critical dimension variations of minimum-sized features which are much smaller than achieved by optical or e-beam lithography. It also provides a doubling of device density for a given lithography pitch. This spacer lithography technology is used to pattern silicon-fin structures for double-gate MOSFETs and CMOS FinFET results are reported.

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1. Introduction

Thin body SOI devices are attractive for scaling CMOS into the nanoscale regime. One of the most promising structures is the FinFET with a double-gate that straddles a narrow silicon fin, which provides an ideal 60 mV/dec subthreshold swing and robustness against short-channel effects [1–3]. The thin body minimizes sub-surface leakage paths between source and drain [4]. Nearly all the leakage current flows along the center of the fin where the electric potential is the least effectively controlled by the gate. Therefore, a thinner body allows for more aggressive gate-length scaling.

For the FinFET, short-channel effects can be suppressed by employing a body thickness (Si-fin width $W_{\text{fin}}$ in Fig. 1, which is a body thickness in the horizontal double gate device) which is approximately half of gate length $L_g$ [2,5]. This is clearly impossible to accomplish with standard lithography technologies when $L_g$ is at the limit of lithography. E-beam lithography has produced 15 nm gates [6] and extreme-ultra-violet (EUV) lithography has generated 38 nm period patterns [7]. But the throughput of e-beam lithography is too low for even research and its uniformity is not yet satisfactory for deep sub-tenth micron gate length fabrication as shown in Fig. 2, and EUV lithography is not readily available yet.

The uniformity of silicon fin width is especially critical for the FinFET because variation in fin width ($W_{\text{fin}}$) can cause a change in channel potential and sub-bands structures, which governs short-channel behavior and quantum confinement effects of inversion charges [8,9]. Also if $L_g / W_{\text{fin}}$ is smaller than 1.5, drain induced barrier lowering (DIBL), subthreshold swing, and off-state leakage current increase significantly [2]. Thus, small change of fin width results in large variation of device characteristics for the short gate lengths. Taller silicon fin ($H_{\text{fin}}$ in Fig. 1) is desirable because it provides a large channel width [10]. A high fin density is also required to obtain large transistor drive current with good layout-area efficiency.

Spacer lithography process technology is attractive for overcoming the limits of conventional lithography techniques in terms of pattern fidelity, critical dimension (CD) variation in Fig. 2, and pattern density. The spacer lithography technology described in this paper can produce extremely narrow and uniform fin widths. One potential drawback of the spacer lithography is that it...
provides only one line width. But by combining a conventional masking process and the spacer process in a novel manner, we overcome this limitation. Silicon fins down to 6.5 nm as shown in Fig. 6(a) are successfully achieved.

2. Device fabrication

Spacer lithography technology provides for a doubling of fin density, which doubles the drive current for a given lithography pitch, as shown in Fig. 3(a) and (b). All masking processes used in this work were performed with I-line optical lithography, because its throughput is much better than e-beam lithography and spacer lithography technology does not require very high resolution lithography. (100) SOI wafers were used as the starting material. The 100 nm silicon film was reduced to 50 nm by thermal oxidation and 4 nm thermal pad oxide was grown to relieve the stress between nitride hard mask and silicon fin. A 50 nm nitride was deposited on the pad oxide serving as a hard mask to protect the silicon fin during the subsequent gate etch. A 200 nm sacrificial Si$_{0.4}$Ge$_{0.6}$ was deposited by LPCVD on the nitride hard mask and patterned (to support the spacers) with optical lithography and plasma etching. A range of 10 nm to 30 nm high temperature oxide (HTO) was then deposited by LPCVD over the patterned sacrificial Si$_{0.4}$Ge$_{0.6}$ layer. The thickness of HTO at the sidewalls of the sacrificial Si$_{0.4}$Ge$_{0.6}$ structures determines the final fin width. An extremely narrow fin width, beyond the lithographic limit, as well as very uniform fin width can therefore be obtained with this spacer lithography process. A subsequent anisotropic HTO spacer dry etch removed the HTO film on top of the sacrificial Si$_{0.4}$Ge$_{0.6}$ structure to generate an even number of spacers. Fig. 2 shows that the spacer technique provides very low CD variation compared to e-beam lithography with SAL-601 resist. Sacrificial Si$_{0.4}$Ge$_{0.6}$ was removed with (5:1:1)
H₂O:NH₄OH:H₂O₂ at 75 °C [11]. HTO, thermally grown oxide, nitride, and silicon were not etched significantly in this solution. The resulting HTO spacer profile is shown in Fig. 4.

Optical lithography was used to define large S/D contact pads as shown in Fig. 5(a). Therefore, the active silicon was patterned with hard mask HTO spacers for the fins and photo-resist for the S/D contact pad regions. One drawback of the spacer technique is that only one line width is provided. However, various and wide fins were achieved by using the photo-resist to define the fins as well as the S/D contact pads as shown in Fig. 5(b). Thereafter, spacers were used for the narrowest fins and the S/D contact pad mask was used for making wide or variable fin widths. Then, anisotropic silicon etching was used to define the silicon active area. Silicon fins as narrow as 6.5 nm were obtained with the spacer lithography technology as shown in Fig. 6(a) and (b).

A sacrificial oxidation step was used to remove the etch damage. A 10 nm of thermal oxide was grown for 12 min at 900 °C with O₂. The sacrificial oxide was removed with diluted HF. Some part of buried oxide was etched and an undercut profile is produced as shown in Fig. 7(b). The gate oxide was grown at 750 °C for 12 min. Si₆₀Ge₄₀ deposited by LPCVD was chosen as the gate material. Planarized gate surface (in the inset of Fig. 7(b)) by CMP produced a large depth of focus (DOF) margin and wide etching window so that
poly-SiGe stringers or residues were removed completely along the fin. A 100 nm gate hard mask oxide by LPCVD was deposited and phosphorous implantation was followed for gate doping. The gate was patterned over the vertical fins by using I-line lithography with a subsequent resist ashing-hard mask oxide trimming technique [12] as shown in Fig. 8(a) and (b). A 20 nm spacer nitride and 10 nm HTO were deposited, thereby, bi-layer spacers were made after spacer etch-back. Masked S/D implantation and RTA (900 °C, 1 min) to make CMOS were followed. Metallization or silicide process was not used in this work and 400 °C H2 annealing was applied.

3. Spacer FinFETs performances

Fig. 9(a) shows that gate current reduces as a fin width decreases because of a reduction of the vertical electric field in thin body SOI as shown in Fig. 9(b) [13].
Fig. 10 shows CMOS subthreshold and drive current characteristics for six-fins transistors defined using spacer lithography. All currents are normalized with $2H_{\text{fin}}$ (fin height or SOI film thickness in Fig. 1 and Fig. 7(b)) per fin, which is a conservative definition of the channel width in the double-gate. Fig. 11 shows $I$–$V$ characteristics of single-fin devices defined by conventional lithography. The relatively low NMOS drive current is due to a degraded electron mobility caused by silicon fin sidewall roughness generated by the dry etch process [14]. This degradation by surface roughness is more severe in NMOS than in PMOS because the inversion charge centroid of electrons is closer to the gate oxide interface than that of holes as shown in Fig. 12. Relatively low drive current in the multi-fin devices caused by higher S/D extension resistance as shown in Fig. 5.

Fig. 13(a) shows that the drive current is strongly affected by extension resistance. Specific test structures were used to investigate the drive current dependence on the series resistance, from the gap $S_2$ between the gate and the edge of source pad as shown in Fig. 8(a). Fig. 13(b) shows that fin resistance is proportional to extension length and extracted doping concentration of fin

Fig. 11. $I$–$V$ characteristics of single-fin device ($L_g = 60$ nm, $W_{\text{fin}} = 40$ nm, and $T_{\text{ox}} = 2.5$ nm). The fins are defined by conventional lithography on the same wafer. (a) Subthreshold $I_d$–$V_g$ characteristics. (b) $I_d$–$V_d$ characteristics.

Fig. 12. Inversion charge centroid of electrons and holes at $V_g - V_t = 0.7$ V. This numerical simulation was performed with Shred [15].
swing and DIBL dependence on the gate length, respectively. These short-channel effects can be suppressed as the fin width reduces. Short-channel effects of PMOS are more than those of NMOS as shown in Fig. 10(a), Fig. 11(a), and Fig. 14 because boron diffusivity in PMOS S/D is larger than phosphorus diffusivity in NMOS S/D for the same RTA condition.

4. Conclusion

A spacer lithography technology is developed for defining narrow silicon fins for double-gate FinFETs. A 6.5 nm wide silicon fin was successfully defined, which is the smallest feature ever reported for silicon structure. This technology provides minimum-sized features beyond the limit of the lithography, better CD uniformity, and twice the device density. Sub-60 nm CMOS FinFETs are demonstrated for the first time and show excellent short-channel behavior due to the double gate structure with a ultra-thin body SOI, which will lead the device scaling beyond sub-10 nm.

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