Optimization of Symmetric Spiral Inductors On Silicon Substrate

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Abstract
Symmetric spiral inductors are used for differential circuit applications for their robustness and superior noise rejection properties. In this work, characteristics of quality factor and inductance of symmetric inductors having octagonal structures, and the methods to improve performance have been suggested using the Agilent Momentum simulator [1]. From the results, we get differential quality-factor of 14.4 at 4.5 GHz with symmetric octagonal inductor with poly PGS.

1. Introduction
One of the key factors that determine the performance of RF integrated circuits (RF IC’s) is the availability of good quality integrated inductors. Unfortunately, parasitic effects, such as coupling capacitance and losses related to the substrate degrade their performance. These unwanted effects are particularly important for silicon substrates [2].

In this paper, the way to design the optimum structure of symmetric spiral inductors for high quality factor is studied. Simulation has been performed to obtain the optimized layout. The Agilent Momentum simulator [1] was used to evaluate the performance of inductors with different layouts.

2. Results and Discussion
Figure 1 shows the top view of a 2-turn (N) symmetric octagonal inductor with variable parameters of metal width (W), metal spacing (S) and inner radius (R) using metal 6 as the top metal and metal 5 as the cross metal. There is symmetry between the two ports, Port1 and Port2. The thickness of the top Al layer was assumed to be 2 µm. Typical process values in 0.18 µm standard CMOS technology are used for all the other process parameters.

Figure 2 shows single-ended and differential Q-factors of symmetric octagonal inductors. Lower parasitics for differential excitation result in a high Q-factor compared with the single-ended connection. The differential circuit topologies are common in integrated circuits because of their robustness and superior noise rejection properties.

Figure 3 shows Q-factor and inductance with different metal spacing. As the metal spacing decreases, the Q-factors increases. Therefore, minimum metal spacing should be used to get maximum Q-factor at given inductance. The typical minimum think-metal spacing for 0.18 µm CMOS technology is 1.5 µm and the value is used in this paper.

Figure 4 shows the inductance and the maximum differential Q-factor as a function of inductor core total length. The inductance of a symmetric octagonal inductor with top metal as Al 2 µm can be expressed as follows :

\[ L_s = (2.8 \times L_{tot}) - 0.1 \]

Where

- \( L_s \) inductance in nH
- \( L_{tot} \) total length of inductor in mm

But Q-factor is varied with fixed inductor core total length due to different series resistance. Figure 5 shows the
frequency dependent series resistances of different number of turn with fixed total length of symmetric octagonal inductor as 1000 µm and 5000 µm. For the case of short inductor core, the proximity effects through the center of spiral and inner turns are dominant. Decrement of N with fixed total length reduces series resistance due to the suppression of proximity effects [3]. For the case of long inductor core, the proximity effects are no longer dominant factor. With fixed core length, DC series resistance is related to the number of turn of the inductor core. As the number of turn increased, DC resistance is increased relatively [4].

Figure 6 and Figure 7 show the inductance and differential Q-factor with various metal width using selected NxRxS pairs from Figure 4. As metal width increases, the inductance decreases slightly due to self-inductance reduction [5], but the differential Q-factor is enlarged due to small series resistance. Increment of metal width cause larger silicon area, which cause the decrement of frequency of maximum Q-factor (F_Qmax) due to larger substrate effects.

Using Figure 7 and the procedure shown in Figure 8, we optimize 5 nH symmetric octagonal inductor on silicon at 4.2 GHz as NxRxWxS = 4x75x10x1.5.

Figure 9 shows the optimized NxRxWxS pairs for each N from 3 to 5. By considering the Q-factor as well as the area of the inductor, NxRxWxS = 4x75x10x1.5 is optimum. The structure has the differential Q-factor of 12.9 at 4.3 GHz and single-ended Q-factor of 8.24 at 2.4 GHz.

Figure 10 shows differential Q-factor, inductance, and out dimension of various shapes of symmetric inductor with optimized NxRxWxS. With same inductance of 5 nH, circular inductor has larger Q-factor due to smaller series resistance. Octagonal inductor is the optimized structure with the view of Q-factor and device dimension.

Figure 11 shows differential Q_{max} and out dimension of optimized structure with various type of stacked metal layer. Stacked layer of M3-M6 represents M3/M4/M5/M6 stacked inductor core with cross metal of M2. As the number of stacked layer increased, the metal width is decreased to optimize at given inductance within operation frequency range. Decrements of metal width cause the increments of series resistance and deterioration of Q-factor.

Figure 12 shows the improvement of Q-factor on poly PGS. The structure with poly PGS shows 11% improvement with differential Q-factor. Table 1 shows the inductance and differential Q_{max} of various type of symmetric inductor on silicon.

Figure 13 compared measured and simulated results with single-ended Q-factor of symmetric square inductor with poly PGS. The total error between measured and simulated Y_{11} was less than 10% with the frequency range of 4.7 GHz. From these results, we conclude that the electromagnetic planar solvers are a powerful tool in the design of RF integrated inductors.

3. Conclusions

In this paper, the optimization of symmetric spiral inductors having octagon structure is presented. The minimum metal spacing should be used to get maximum Q-factors. The way to maximize Q-factor at fixed total length by controlling R or N was also addressed. The procedure to optimize the layout parameters is shown. Single metal layered (M6), octagonal symmetric inductor with PGS shows maximized differential Q-factor at given inductance and frequency range. The optimized layout parameter of 5 nH / 4.2 GHz symmetric octagonal inductor with M6 is 4x75x10x1.5 with PGS, which has differential Q-factor of 14.4 at 4.5 GHz.
Acknowledgment
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References
Fig. 5 Series resistance versus number of turns of symmetric octagonal inductor with fixed total length of 1 mm and 5 mm.

Fig. 6 Inductance and differential maximum Q-factor versus metal width of symmetric octagonal inductor with optimized NxRxS pairs.

Fig. 7 Inductance, differential Qmax, and FQmax of symmetric octagonal inductor with different metal width, with fixed NxRxS of 4x75x1.5.

Fig. 8 Procedure of inductor layout optimization.

Fig. 9 Differential Q-factor and inductance as a parameter of number of turns with optimized RxWxS.

Fig. 10 Differential Q-factor, inductance, and out dimension as a parameter of symmetric inductor shape with optimized NxRxWxS.
Table 1 Comparison of inductance and differential quality-factor for optimized layout parameters

<table>
<thead>
<tr>
<th>PGS</th>
<th>Symmetric Inductor on Silicon</th>
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<tbody>
<tr>
<td></td>
<td>Without PGS</td>
</tr>
<tr>
<td>Stacked Metal Layer</td>
<td>M6</td>
</tr>
<tr>
<td>Shape</td>
<td>Square</td>
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<tr>
<td>NxRxWxS</td>
<td>4x65x10x1.5</td>
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Fig. 11 Differential Q_{\text{max}} and optimized metal width from the procedure with number of stacked metal layer.

Fig. 12 Effect of poly PGS on differential Q-factor and inductance with symmetric octagonal inductor.

Fig. 13 Measured and simulated single-ended Q-factors of symmetric square inductor with poly PGS.