Curriculum Vitae

Wu-Kang Kim, Ph. D

Post-Doctoral Researcher - Nano-Oriented Bio-Electronics Lab
Supervisor : Yang-Kyu Choi
Dept. of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST)
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M.S., Ph. D., Post-Doctoral Researcher - Takagi-Takenaka Group
Supervisor : Shinichi Takagi
Dept. of Electrical Engineering, Graduate School of Engineering, The University of Tokyo
Room No.460, Electrical Dept. Bldg. No.10, Yayoi, Bunkyo-ku, Tokyo, Japan, 〒113-0032
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RESEARCH INTERESTS

Electronics Engineering : Next Generation Electronics

- Advanced transistors
  - Next generation (Group 4 or III-V) MOSFETs
  - Tunneling FETs
  - Fin-FETs
  - 2-Dimentional Materials
  - Vertical FETs
- Semiconductor Technology development
  - Ge condensation
  - Wafer bonding
  - Strain technology
  - Channel engineering, S/D formation technology
  - Doping, CMOS, Semiconductor physics, nano-electronics
- Other applications
  - Synaptic devices for Neuromorphic application
  - Next generation flash memory devices
  - Nano-Electro Mechanical Switch by Physical Unclonable Function (PUF)

EDUCATION

The University of Tokyo

2014. 4 – 2017. 9 The University of Tokyo (Japan)
Ph.D., Dept. of Electrical Engineering. Graduate School of Engineering

2012. 4 – 2014. 3 The University of Tokyo (Japan)
M.S. Dept. of Electrical Engineering. Graduate School of Engineering

Nagoya University

2008. 4 – 2012. 3 Nagoya University (Japan)
B.S., Electrical and Electronic Engineering and Information Engineering,
School of Engineering

High Schools

2005. 1 – 2007. 2 Anyang Foreign Language High School (Korea)
Major in natural science and English

2004. 1 – 2005. 1 Fort Lee High School (NJ, USA)

RESEARCH EXPERIENCE AND TRAINING

2018. 04 – *present* **Post-Doctoral Researcher**, Korea Institute of Science and Technology
Research on Post-Si MOSFETs, Neuromorphic devices, DRAM, Flash memory
Supervisor : Yang-Kyu Choi

2017. 10 – 2018. 03 **Post-Doctoral Researcher**, The University of Tokyo
Research on sub-5 nm thick Ge-on-Insulator MOSFET
Supervisors : Shinichi Takagi, Mitsuru Takenaka

2014. 4 – 2017. 9 **Graduate Student Researcher**, The University of Tokyo
Thesis : "Study on performance enhancement of ultra-thin-body Ge-on-Insulator pMOSFETs by Ge condensation method"
Supervisor s : Shinichi Takagi, Mitsuru Takenaka

2012. 4 - 2014. 3 **M.S. Researcher**, The University of Tokyo
Thesis: "Sb-diffused source and drain ultra-thin body Ge-On-Insulator nMOSFETs fabricated by Ge condensation technique"
Supervisor : Shinichi Takagi, Mitsuru Takenaka

2014.10 - 2015.3 **Teaching Assistant** , The University of Tokyo
Understanding and evaluating MOSFETs (A class for undergraduate students)

SKILLS

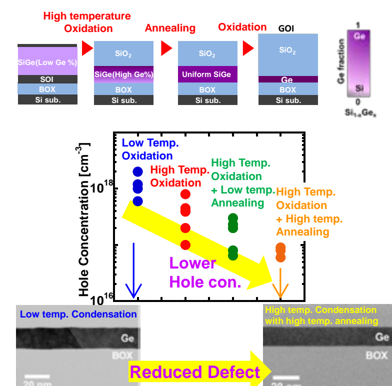
Simulation : TCAD (Sentaurus)
Fabrication : CMOS fabrication methods (Condensation, Diffusion, Wafer bonding, diffusion, SOG, CVD, RIE, ALD, Annealing, Lithography, etc.)
Estimation : Over all Electrical characterization, Hall measurement, Raman spectroscopy, Photo Luminescent, Spectroscopic Ellipsometry, AFM, TEM, etc.
Language : Korean, English, Japanese

MAJOR ACHIEVEMENTS

Ge-on-Insulator Channel improvement

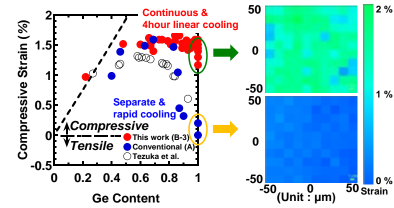
1. Reduction of defects in GOI

GOI (Ge-on-insulator) is known to be one of the most promising structures to overcome physical limitations of further scaling, with both high hole and electrical mobility, as well as ability to suppress short channel effect. Among the GOI fabrication methods, Ge condensation method has great potential with easy process and ability to form ultra-thin body GOI layers. However, one of the problems to the Ge condensation was high hole concentration, due to defect and vacancy, generated during the process. I have reduced the hole concentration and reduced defect with new optimized Ge condensation method by diffusion Ge into SiGe layer during the process using high temperature oxidation and annealing in-between the oxidation processes.



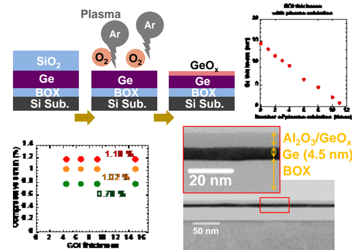
2. Strain application to GOI

Another problem to the Ge condensation was the strain relaxation during the Ge condensation process. Strain relaxation not only caused defect on the crystalline but also made it impossible to enhance with strain application to the Ge channel. I have successfully analyzed one of the most dominant reasons for the strain relaxation during the Ge condensation process and also suppressed strain relaxation to achieve ~1.6 % compressive strain to GOI layer.



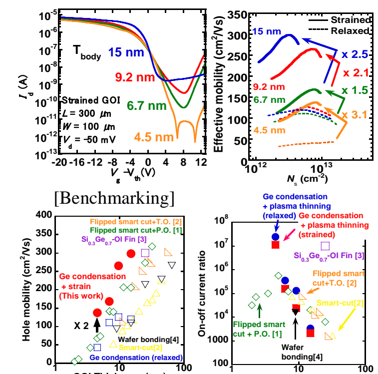
3. Sub 5-nm-thick strained GOI layer fabrication

Achieving GOI thickness less than 5 nm is very important, not only for the suppression of short channel effect to the upcoming scaled GOI MOSFETs, but also with the potential of fully-depleted MOSFETs. I have established a digitally thinning method using plasma oxidation. This resulted in very uniform GOI layers with thickness less than 5 nm with very good uniformity, even with the top-down process. Moreover this enabled thinning and forming sub 5 nm thick GOI layer with compressive strain for the first time.



4. Performance enhancement on GOI pMOSFETs

The significance of forming a strained GOI is lowering effective mass which leads to higher pMOSFET performance. With the strained GOI layers, fabricated by Ge condensation, I have enhanced GOI pMOSFET performance over twice of compared to conventional methods. Record high hole mobility has been achieved in sub 15-nm thick GOIs. In addition, the thinning method enabled me to lower leak current in 4.5 nm-thick GOI layer to achieve on-off current ratio over 10^7, which is even higher than device with fin-FETs[3].



[1] Yu et al., IEDM (2015) [2] X. Yu et al., Micro Electron Eng. (2015) [3] Hashemi et al., VLSI symp., (2015) [4] C. H. Lee et al., SOI Conf., (2011)

PUBLICATIONS

- *Papers*

1. **W.-K. Kim**, K. Kuroda, M. Takenaka and S. Takagi, "Sb-Doped S/D Ultrathin Body Ge-on Insulator nMOSFET fabricated by Improved Ge condensation Process", IEEE Transactions on Electron Devices, **61**, 10, p. 3379 (Oct. 2014)
2. **W.-K. Kim**, M. Takenaka and S. Takagi, "Properties of ultrathin-body condensation Ge-on-insulator films thinned by additional thermal oxidation", Japanese Journal of Applied Physics, **54**, 04DA05 (Feb. 2015)
3. M. Seo, M.-H. Kang, S.-B. Jeon, H. Bae, J. Hur, B.-C. Ja S. Yun, S. Cho, **W.-K. Kim**, K.-M, Hwang, S. Hong, S.-Y, Choi, and Y.-K. Choi, "First Demonstration of a Logic-process Compatible Junctionless Ferroelectric FinFET synapse for Neuromorphic Applications", IEEE Electron Device Letters, (Jul. 2018)

- *International Conference*

1. **W.-K. Kim**, Y.-F. Kin, Y. Kim, S.-H. Kim, T. Osada, M. Hata, M. Takenaka and S. Takagi, "Sb-diffused Source/Drain Ultrathin body Ge-on insulator nMOSFETs fabricated by Ge condensation", SSDM (Sep. 2013) p. 744-745
2. [Invited paper]S. Takagi, S.-H. Kim, M. Yokoyama, **W.-K. Kim**, R. Zhang and M. Takenaka, "Ultra-thin body MOS device technologies using high mobility channel materials", IEEE SOI-3D-Subthreshold Microelectronics

Technology Unified Conference, Hyatt Regency Monterey Hotel and Spa, Monterey, California, October 7-10 (Oct. 2013)

3. **W.-K. Kim**, M. Takenaka and S. Takagi, "Properties of ultrathin body condensation GOI films thinned by additional thermal oxidation" SSDM (Sep. 2014) p. 34-35
4. S. Takagi, **W.-K. Kim,** X. Yu, J.-H. Han, R. Zhang, and M. Takenaka, "Ge/SiGe CMOS device technology for future logic LSIs," E-MRS Spring meeting 2015, symposium K, Transport and photonics in group IV-based nanodevices, Lille (France), (May 2015)
5. **W.-K. Kim**, M. Takenaka and S. Takagi, "High Performance 4.5-nm-Thick Compressively-Strained Ge-on-Insulator pMOSFETs Fabricated by Ge Condensation with Optimized Temperature Control," Symp. On VLSI technology, T123 (June 2017) p. 34-35
6. K.-W. Jo, **W.-K, Kim**, M. Takenaka and S. Takagi, "Effect of SiGe Layer Thickness in Starting Substrate on Electrical Properties of Ultrathin Body Ge-on-Insulator pMOSFET fabricated by Ge Condensation", presented at International Conference on Solid State Devices and Materials, (Sep. 2017)
7. K.-W. Jo, **W.-K, Kim**, M. Takenaka and S. Takagi, "Hole Mobility Enhancement in Extremely-Thin-Body Strained GOI and SGOI pMOSFETs by Improved Ge Condensation Method", Symp. On VLSI technology, T18-3 (May. 2018)

- *Domestic Conference in Japan*

1. **W.-K. Kim**, Y.-F. Kin, Y. Kim, S.-H. Kim, T. Osada, M. Hata, M. Takenaka and S. Takagi, "Ultra-thin body Ge-on insulator nMOSFETs fabricated by Ge condensation and Sb diffusion", JSAP Autumn (Sep. 2013)
2. **W.-K. Kim**, Y.Kim, S.-H. Kim, T. Osada, M. Hata, M. Takenaka and S. Takagi, "Ultra-thin body Ge-on insulator nMOSFETs by Ge condensation and Sb-diffused source/drain", JSAP Spring (March. 2014)
3. **W.-K. Kim**, M. Takenaka and S. Takagi, "Effects of thinning condensation UTB GOI films by additional thermal oxidation", JSAP Autumn (Sep. 2014)
4. **W.-K. Kim**, M. Takenaka and S. Takagi, "Compressively-strained ultra-thin body Ge-OI structure fabricated by Ge condensation method with reduced temperature cycles", JSAP Spring (March. 2016)
5. **W.-K. Kim**, M. Takenaka and S. Takagi, "Effect of cooling process on compressive strain in GOI layers fabricated by Ge condensation", JSAP Spring (March. 2017)
6. **W.-K. Kim**, M. Takenaka and S. Takagi, "High compressive strain GOI pMOSFET fabricated by Ge condensation process with reduced cooling rate", JSAP Autumn (Sep. 2017)
7. **W.-K. Kim**, M. Takenaka and S. Takagi, "Extremely-thin-body strained GOI pMOSFETs fabricated by thinning Ge condensation GOI through plasma oxidation", JSAP Autumn (Sep. 2017)
8. K.-W. Jo, **W.-K. Kim**, M. Takenaka and S. Takagi, "Effect of SiGe Layer Thickness in Starting Substrate on Electrical Properties of Ultrathin Body Ge-on-insulator pMOSFET fabricated by Ge Condensation", JSAP Autumn (Sep. 2017)

HONORS AND AWARDS

Awards

IEEE EDS Japan Chapter Student Award	2018. 2.
Japanese Journal of Applied Physics, 42nd Presentation Award, JSAP Spring**,** 16p-412-14	2017. 9.
Best Student Experiment Award	2011. 2.

Scholarships

Tokyu Foundation Scholarship	2016. 4 –2017.9
Doctoral Student Special Incentives, Graduate School of Engineering, The University of Tokyo	2014. 4 –2016.3
The University of Tokyo FUND scholarship	2013.9 – 2014.3
Korea-Japan Government Joint Scholarship	2008.4 – 2012.3