Jae Hur

PERSONAL INFORMATION

- Date of Birth: 11th August, 1989
- Nationality: South Korea
- Address: 291 Daehak-ro, Yuseong-gu, Daejeon, 34141, Republic of Korea
- Mobile: +82-10-9445-0736
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EDUCATION

- **Ph.D. Candidate in Electrical Engineering**
  Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea
  Academic Advisor: Prof. Yang-Kyu Choi — Feb. 2015 − Present
- **M.S. in Electrical Engineering**
  Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea
  Academic Advisor: Prof. Yang-Kyu Choi — Feb. 2013 − Jan. 2015
- **B.S. in Electrical Engineering**
  Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea
  Academic Advisor: Prof. Seung-Tak Ryu — Mar. 2009 − Jan. 2013

RESEARCH INTEREST

- Neuromorphic system and devices
- Modeling and Simulation for nanometer-scale electronic device
- Fabrication and Characterization for nanometer-scale electronic device

(nanometer-scale electronic device includes: Tunnel FET, Vertically integrated FET, Schottky barrier FET, BJT, Charge-plasma FET *etc*.)

- Semiconductor-based reconfigurable antenna

RESEARCH PROJECT

- **Project** sponsored by KAIST
  (Title : Artificial Intelligence Semiconductor Devices and Integrated Circuits)
  May. 2018 − Present
- **Project**: Industrial-University Cooperation Research with Samsung Electronics
  (Title : DRAM memory based on vertical Ge biristor with gateless and capacitorless structure)
  Nov. 2015 − Present
- **Project** sponsored by the Ministry of Science and ICT as Global Frontier Project
  (Title : Ultra-low power hybrid electronic device)
  Sep. 2015 − Present
- **Project**: Industrial-University Cooperation Research with Samsung Electronics
  (Title : Investigation of Gate-All-Around Tunneling FET)
  Jul. 2015 − Present
- **Project** sponsored by Electronics and Telecommunications Research Institute
  (Title : Development on semiconductor based smart antenna for future mobile communications)
  Mar. 2015 – Feb. 2018
- **Project**: Industrial-University Cooperation Research with Samsung Electronics
  (Title : Dopant segregated metal-silicide S/D for 3D stack memory and logic device)

Jul. 2013 − Jun. 2014

EDUCATIONAL EXPERIENCE

- **Teaching Assistant**: Introduction to VLSI Devices, Prof. Yang-Kyu Choi, Spring semester, 2017.
- **Teaching Assistant**: Semiconductor Memory and SoC Technology, Samsung executives and Prof. Yang-Kyu Choi, Fall semester, 2016.
- **Teaching Assistant**: Laboratory Experiment, Prof. Yang-Kyu Choi, Spring semester, 2016.
- **Teaching Assistant**: Semiconductor Device, Prof. Hyun-Joo Lee, Fall semester, 2015.
- **Teaching Assistant**: Semiconductor Device, Prof. Yang-Kyu Choi, Spring semester, 2015.
- **Teaching Assistant**: Advanced MOS Technology, Prof. Yang-Kyu Choi, Fall semester, 2014.
- **Teaching Assistant**: Laboratory Experiment, Prof. Yang-Kyu Choi, Spring semester, 2014.
- **Lecturer**: Python Language Lab, Aklan state University Ibajay campus, Voluntary Service of Korea IT Volunteers in the Philippines, Jul. − Aug. 2011.

QUALIFICATIONS AND SKILLS

- Experience with CMOS device fabrication equipments including RIE, Deep RIE, KrF scanner, CMP, RTP, Aligner, Furnace, Sputter, Dry/wet etching, and *etc*.
- Numerical computation and data analysis experience with MATLAB, LabView, Origin, and Python.
- Device and process simulation experience with TCAD, ATLAS, ATHENA.
- Layout experience with Cadence.
- Analysis equipments including In-line CD-SEM, FB-SEM, AFM, FIB, and TEM.

HONORS AND AWARDS

- **Full Scholarship for Undergraduate Students** in Korea Advanced Institute of Science and Technology. 2009 − 2012
- **Full Scholarship for Graduate Students** in Korea Advanced Institute of Science and Technology. 2012 − Present
- **Grand Prize (Kim, Choong-Ki Scholarship) for Top 2 student** among the Ph.D. students in School of Electrical Engineering (KAIST) Apr. 2015
- **Grand Prize (Kim, Choong-Ki Scholarship) for Top 2 student** among the Ph.D. students in School of Electrical Engineering (KAIST) Apr. 2016
- **Grand Prize (Kim, Choong-Ki Scholarship) for Top 2 student** among the Ph.D. students in School of Electrical Engineering (KAIST) Apr. 2017
- **Best Poster Paper Award in the 2015 IEEE Nano**, Byung-Hyun Lee, Min-Ho Kang, **Jae Hur**, Dae-Chul Ahn, Dong-Il Lee, Hagyoul Bae, and Yang-Kyu Choi (Title : An optimimum strategy for low voltage operation of the mechanical switch) Aug. 2015
- **Samsung Humantech Bronze Award**, Hagyoul Bae, Daewon Kim, **Jae Hur**, and Yang-Kyu Choi Jan. 2015

ACTIVITY

- Golden List of Reviewers of ***IEEE Transactions on Electron Devices*** 2017, 2016
- Golden List of Reviewers of ***IEEE Electron Device Letters*** 2016
- Reviewer of ***IEEE Electron Device Letter*** 2016 − Present
- Reviewer of ***IEEE Transactions on Electron Devices*** 2016 − Present
- Reviewer of ***IEEE Transactions on Nanotechnology*** 2017 − Present
- Reviewer of ***Nanotechnology*** 2018 − Present
- Reviewer of ***Solid-State Electronics*** 2016 − Present
- Reviewer of ***Semiconductor Science and Technology*** 2016 − Present
- Reviewer of ***Journal of Semiconductor Technology and Science*** 2016 − Present

- Reviewer of ***Electronics Letters*** 2016 − Present
- Reviewer of ***Micro and Nano Letters*** 2018 − Present

PUBLICATIONS–24 Papers (List by reversed chronological order)

[1st author – 6 papers except manuscripts under review**]**

- **Jae Hur***, Byung Chul Jang*, Jihun Park, Dong-Il Moon, Hagyoul Bae, Jun-Young Park, Gun-Hee Kim, Seung-Bae Jeon, Myungsoo Seo, Sungho Kim, Sung-Yool Choi, and Yang-Kyu Choi, "A Recoverable Synapse Device Using a Three-dimensional Silicon Transistor", *Advanced Functional Materials*, Oct. 2018. (*These authors equally contributed to this work.), **Accepted**. **[PDF]**
- **Jae Hur***, In-Joong Nam*, Young-Kyun Cho*, Da-Jin Kim, Soo-Bean Cho, Eon-Seok Jo, Choong-Ki Kim, Geon-Beom Lee, Cheol Ho Kim, Seok Bong Hyun, Dongho Kim, and Yang-Kyu Choi, "Semiconductor Antenna: Future of Beamforming Antenna Using Vertical PIN Diode Array", *Nature Communications*, Oct. 2018. (*These authors equally contributed to this work.), **Submitted**.
- **Jae Hur**, Woo Jin Jeong, Mincheol Shin, and Yang-Kyu Choi, "Schottky Tunneling Effects in a Tunnel FET", *IEEE Transactions on Electron Devices*, Oct. 2017. **[PDF]**
- **Jae Hur**, Dong-Il Moon, Jin-Woo Han, Gun-Hee Kim, Chang-Hoon Jeon, and Yang-Kyu Choi, "Tunneling Effects in a Charge-Plasma Dopingless Transistor", *IEEE Transactions on Nanotechnology*, Mar. 2017. **[PDF]**
- **Jae Hur**, Byung-Hyun Lee, Min-Ho Kang, Dae-Chul Ahn, Tewook Bang, Seung-Bae Jeon, and Yang-Kyu Choi, "Comprehensive Analysis of Gate-induced Drain Leakage in Vertically Stacked Nanowire FETs: Inversion-mode versus junctionless mode", *IEEE Electron Device Letters*, May. 2016. **[PDF]**
- **Jae Hur**, Ji-Min Choi, Jong-Ho Woo, Hyunjae Jang, and Yang-Kyu Choi, "A Generalized Threshold Voltage Model of Tied and Untied Double-gate Junctionless FETs for a symmetric and asymmetric structure", *IEEE Transactions on Electron Devices*, Sep. 2015. **[PDF]**
- **Jae Hur**, Dong-Il Moon, Ji-Min Choi, Myeong-Lok Seol, Ui-Sik Jeong, Chang-Hoon Jeon, and Yang-Kyu Choi, "A Core Compact Model for Multiple-gate Junctionless FETs", *IEEE Transactions on Electron Devices*, Jul. 2015. **[PDF]**

[Co-author – 18 papers except manuscripts under review**]**

- Seung-Wook Lee, Seong-Yeon Kim, Kyu-Man Hwang, Ik-Kyeong Jin, **Jae Hur**, Do-Hyun Kim, Wu-Kang Kim, and Yang-Kyu Choi, "A Comprehensive Study of a Single Transistor Latch in Vertical Pillar-Type FETs with Asymmetric Source and Drain", *IEEE Electron Device Letters*, Sep, 2018. **Accepted**. **[PDF]**
- Da-Jin Kim*, Eon-Seok Jo*, Young-Kyun Cho*, **Jae Hur**, Choong-Ki Kim, Cheol Ho Kim, Bonghyuk Park, Dongho Kim, and Yang-Kyu Choi, "A Frequency Reconfigurable Dipole Antenna with Solid-state Plasma in Silicon", *Scientific Reports*, Sep. 2018. (*These authors equally contributed to this work.), **Accepted**.
- Myungsoo Seo, Min-Ho Kang, Seung-Bae Jeon, Hagyoul Bae, **Jae Hur**, Byung Chul Jang, Seokjung Yun, Seongwoo Cho, Wu-Kang Kim, Myung-Su Kim, Kyu-Man Hwang, Seungbum Hong, Sung-Yool Choi, and Yang-Kyu Choi, "First Demonstration of a Logic-Process Compatible Junctionless Ferroelectric FinFET Synapse for Neuromorphic Applications", *IEEE Electron Device Letters*, Jul. 2018. **[PDF]**
- Gun-Hee Kim, Yong-Yoon Kim, Hagyoul Bae, **Jae Hur**, Choong-Ki Kim, Tewook Bang, Yun-Ik Son, Seong-Wan Ryu, and Yang-Kyu Choi, "Highly Biased Linear Condition Method for Separately Extracting Source and Drain Resistance in MOSFETs", *IEEE Transactions on Electron Devices*, Feb. 2018. **[PDF]**
- Seong-Yeon Kim, Byung-Hyun Lee, **Jae Hur**, Jun-Young Park, Seung-Bae Jeon, Seung-Wook Lee, and Yang-Kyu Choi, "A Comparative Study on Hot-Carrier Injection in 5-story Vertically Integrated GAA MOSFETs", *IEEE Electron Device Letters*, Jan. 2018. **[PDF]**
- Jun-Young Park, **Jae Hur** and Yang-Kyu Choi, "Demonstration of a Curable Nanowire FinFET Using Punchthrough Current to Repair Hot-Carrier Damage", *IEEE Electron Device Letters*, Dec. 2017. **[PDF]**
- Da-Jin Kim*, Jang-Soon Park*, Cheol Ho Kim*, **Jae Hur**, Choong-Ki Kim, Young-Kyun Cho, Jun-Bong Ko, Bonghyuk Park, Dongho Kim, and Yang-Kyu Choi, "Reconfigurable Yagi-Uda antenna based on a silicon

reflector with a solid-phase plasma", *Scientific Reports*, Dec. 2017. (*These authors equally contributed to this work.). **[PDF]**

- Hagyoul Bae, Tewook Bang, Choong-Ki Kim, **Jae Hur**, Seyeob Kim, Chang-Hoon Jeon, Jun-Young Park, Dae-Chul Ahn, Gun-Hee Kim, Yunik Son, Jae-Hoon Lee, Yong-Taik Kim, Seong-Wan Ryu, and Yang-Kyu Choi, "Improved Technique for Extraction of Effective Mobility by Considering Gate Bias-Dependent Inversion Charges in a Floating-Body Si/SiGe pMOSFET", *Journal of Nanoscience and Nanotechnology*, May. 2017. **[PDF]**
- Dongil Lee, Byung-Hyun Lee, Jinsu Yoon, Dae-Chul Ahn, Jun-Young Park, **Jae Hur**, Myung-Su Kim, Seung-Bae Jeon, Min-Ho Kang, Kwanghee Kim, Meehyun Lim, Sung-Jin Choi, and Yang-Kyu Choi, "Three-Dimensional Fin-Structured Semiconducting Carbon Nanotube Network Transistor", *ACS nano*, Nov. 2016. **[PDF]**
- Dae-Chul Ahn, Byung-Hyun Lee, Min-Ho Kang, **Jae Hur**, Tewook Bang, and Yang-Kyu Choi, "Impact of Crystalline Damage on a Vertically Integrated Junctionless Nanowire Transistor", *Applied Physics Letters*, Oct. 2016. **[PDF]**
- Chang-Hoon Jeon, Jun-Young Park, Myeong-Lok Seol, Dong-Il Moon, **Jae Hur**, Hagyoul Bae, Seung-Bae Jeon, and Yang-Kyu Choi, "Joule Heating to Enhance the Performance of a Gate-All-Around Silicon Nanowire Transistor", *IEEE Transactions on Electron Devices*, Jun. 2016. **[PDF]**
- Ui-Sik Jeong, Choong-Ki Kim, Hagyoul Bae, Dong-Il Moon, Tewook Bang, Ji-Min Choi, **Jae Hur**, and Yang-Kyu Choi, "Investigation of Low-frequency Noise in Nonvolatile Memory Composed of a Gate-all-around Junctionless Nanowire FET", *IEEE Transactions on Electron Devices*, May. 2016. **[PDF]**
- Byung-Hyun Lee, **Jae Hur**, Min-Ho Kang, Tewook Bang, Dae-Chul Ahn, Dongil Lee, Kwang-Hee Kim, and Yang-Kyu Choi, "A Vertically Integrated Junctionless Nanowire Transistor", *Nano Letters*, Feb. 2016. **[PDF]**
- Choong-Ki Kim, Chan Hak Yu, **Jae Hur**, Hagyoul Bae, Seung-Bae Jeon, Hamin Park, Yong Min Kim, Kyung Cheol Choi, Yang-Kyu Choi, Sung-Yool Choi, "Abnormal Electrical Characteristics of Multi-layered MoS2 FETs Attributed to Bulk Traps", *2D Materials*, Feb. 2016. **[PDF]**
- Dae-Chul Ahn, Myeong-Lok Seol, **Jae Hur**, Dong-Il Moon, Byung-Hyun Lee, Jin-Woo Han, Jun-Young Park, Seung-Bae Jeon, and Yang-Kyu Choi, "Ultra-Fast Erase Method of SONOS Flash Memory by Instantaneous Thermal Excitation", *IEEE Electron Device Letters*, Feb. 2016. **[PDF]**
- Byung-Hyun Lee, Min-Ho Kang, Dae-Chul Ahn, Jun-Young Park, Tewook Bang, Seung-Bae Jeon, **Jae Hur**, Dongil Lee, and Yang-Kyu Choi, "Vertically Integrated Multiple Nanowire Field Effect Transistor", *Nano Letters*, Nov. 2015. **[PDF]**
- Myeong-Lok Seol, Jong-Ho Woo, Seung-Bae Jeon, Daewon Kim, Sang-Jae Park, **Jae Hur**, and Yang-Kyu Choi, "Vertically Stacked Thin Triboelectric Nanogenerator for Wind Energy Harvesting", *Nano Energy*, May. 2015. **[PDF]**
- Myeong-Lok Seol, Jong-Ho Woo, Dong-Il Lee, Hwon Im, **Jae Hur**, and Yang-Kyu Choi, "Nature-Replicated Nano-in-Micro Structures for Triboelectric Energy Harvesting", *small*, Jul. 2014. **[PDF]**
- Hagyoul Bae, Byung-Hyun Lee, Jun-Young Park, **Jae Hur**, Da-Jin Kim, Myung-Su Kim, Choong-Ki Kim, and Yang-Kyu Choi, "First Demonstration of Gateless and Capacitorless Vertical Type Germanium Biristor for High Density and Low Voltage Memory Application", *IEEE Electron Device Letters*, Oct, 2017. **Submitted**.
- Jun Woo Son, **Jae Hur**, Wu-Kang Kim, Geon-Beom Lee, and Yang-Kyu Choi, "An Optimization Strategy for Low-Operation Voltage Silicon Biristor", *IEEE Transactions on Electron Devices*, Oct, 2017. **Submitted**.

INTERNATIONAL CONFERENCE (List by reversed chronological order)

[6 papers except manuscripts under review**]**

- **Jae Hur**, Choong-Ki Kim, Da-Jin Kim, Tewook Bang, Yang-Kyu Choi, Young-Kyun Cho, Cheol Ho Kim, Bonghyuk Park, Jang-Soon Park, and Dongho Kim, "Silicon-Based Yagi-Uda Antenna Reflector", *International Conference on Electronics, Information, and Communications (ICEIC) 2017*, Jan. 2017. **[PDF]**
- Cheol Ho Kim, **Jae Hur**, Young-Kyun Cho, Bonghyuk Park, and Yang-Kyu Choi, "Experimental Analysis on

RF Conductivity of Surface PIN Diode Arrays for Reconfigurable Silicon Plasma Antennas", *ISMOT 2017*, Jul. 2017.

- Eon-Seok Jo, Dongho Kim, **Jae Hur**, Da-Jin Kim, Choong-Ki Kim, Yang-Kyu Choi, Seok-Bong Hyun, Bong Hyuck Park, Young-Kyun Cho, and Cheol-Ho Kim, "A Frequency Reconfigurable Slot Dipole Antenna using Surface PIN Diodes", *ISAP 2017*, 2017.
- Da-Jin Kim, Tewook Bang, **Jae Hur**, Choong-Ki Kim, Yang-Kyu Choi, Cheol Ho Kim, and Bonghyuk Park, "Optimization of the Intrinsic Length of a PIN Diode for a Reconfigurable Antenna", *International Conference on Electronics, Information, and Communications (ICEIC) 2016*, Jan. 2016. **[PDF]**
- Byung-Hyun Lee, Min-Ho Kang, **Jae Hur**, Dae-Chul Ahn, Dong-Il Lee, Hagyoul Bae, and Yang-Kyu Choi, "An Optimum Strategy for the Low Voltage Operation of the Mechanical Switch", *Nanotechnology (IEEE-NANO), 2015 IEEE 15th International Conference on*, Jul. 2015. **[PDF]**
- Chan Hak Yu, Choong-Ki Kim, **Jae Hur**, Yang-Kyu Choi and Sung-Yool Choi, "Low-Frequency Noise in Hysteresis-Free Multilayer MoS2 FETs", *International Conference on Electronics, Information, and Communications (ICEIC) 2015*, Jan. 2015.

DOMESTIC CONFERENCE (List by reversed chronological order)

[1 papers]

- Tewook Bang, Hagyoul Bae, Choong-Ki Kim, **Jae Hur**, Jun-Young Park, Dae-Chul Ahn, Gun-Hee Kim, Yun-Ik Son, Jae-Hoon Lee, Yong-Taik Kim, and Yang-Kyu Choi, "Improved Split C-V Technique for Accurate Extraction of Mobility by Considering Effective Inversion Charges in p-Channel $Si_{0.8}Ge_{0.2}$ MOSFET," *The 23th Korean Conference on Semiconductors (KCS)*, Feb. 2016.

PATENTS

- Yang-Kyu Choi, Jun Woo Son, **Jae Hur**, "Two-terminal biristor with poly-scrystalline silicon emitter electrode and method for manufacturing thereof," Korean Patent Application no. 10-2018-0096846, Aug. 2018.
- Yang-Kyu Choi, Jun-Young Park, **Jae Hur**, "The local thermal annealing method for curing of gate oxide damage utilizing punchthrough current in MOSFET," Korean Patent Application no. 10-2018-0044236, Apr. 2018.
- Yang-Kyu Choi, Da-Jin Kim, **Jae Hur**, Tewook Bang, Choong-Ki Kim, "Memory device including serially connected pin diodes and fabrication method thereof," Korean Patent Application no. 10-2017-0164949, Nov. 2017.
- Yang-Kyu Choi, **Jae Hur**, "The neuromorphic synapse device based on semiconductor channel including a trap-rich layer," Korean Patent Application no. 10-2017-0139177, Oct. 2017.
- Yang-Kyu Choi, Dong-Il Moon, Ui-Sik Jeong, **Jae Hur**, "Vertically stacked silicon nanowire transistors and fabrication method," Korean Patent Registration no. 10-1783403-0000, Sep. 2017.
- Yang-Kyu Choi, **Jae Hur**, Da-Jin Kim, Choong-Ki Kim, Tewook Bang, "Semiconductor plasma structure and method to fabricate the device," Korean Patent Registration no. 10-1766612-0000, Aug. 2017.
- Yang-Kyu Choi, Dae-Chul Ahn, **Jae Hur**, Jun-Young Park, Dong-Il Moon, "Memory device of supporting fast operation speed and self healing," Korean Patent Registration no. 10-1731183-0000, Apr. 2017.

EQUIPMENT and SIMULATION TOOL

- Silvaco ATLAS Device Simulation Software
- Silvaco ATHENA Device Process Software
- Synopsys Device Simulation Software
- MATLAB, Origin, LabView Software (Numerical computation and data analysis)
- Python language
- Cadence OrCAD (Software Tool for mask layout)
- MA6, MJB4 (Photolithography)

- ICP Asher, Spin Coater, Wet-Station
- Evaporator, Sputter
- Furnace (Oxidation, Annealing)
- Atomic-Force Microscopy (AFM)
- Scanning Electron Microscope (SEM)
- Agilent 4156C / 4145B Semiconductor Parameter Analyzer
- HP 4294A Precision Impedance Analyzer / HP 4284A High Precision LCR Meter
- Keithley 4200-SCS dc voltage sweeper/4225-PMU pulse generator/4225-RPM remote amplifier (switches)
- SR 570 Low-Noise Current Amplifier
- Experience with national nanofab center **[Link]** for fabrication of FinFET, semiconductor antenna, and various types of MOSFETs using equipment list of
  1) EVG6500 from EV Group (Photolithography)
  2) ICP380 etcher from Oxford (Dry etcher)
  3) P-5000 from AMAT (PECVD)
  4) G-1510 from Excelis (Ion-implantation)
  5) RTA200H-SP1 from New Young M Tech (Rapid thermal annealing)
  6) SRN-110 from SORONA (sputter)

and so on.

Reference

- Prof. Yang-Kyu Choi (academic advisor)
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- E-mail: ykchoi@ee.kaist.ac.kr