

Hagyoul Bae

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Korea Advanced Institute of Science and Technology (KAIST)
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EDUCATION AND TRAINING

- **Ph.D in Electrical Engineering** March. 2014– Present
Korea Advanced Institute of Science and Technology (KAIST) Daejeon, Korea
Academic Advisor : Prof. Yang-Kyu Choi
- **M.S. in Electrical Engineering** March. 2009– 2011
Kookmin Univeristy Seoul, Korea
Academic Advisor : Prof. Dong Myong Kim
- **B.S. in Electrical and Electronic Engineering** March. 2003– Feb. 2007
Kookmin University Seoul, Korea

AWARD & SCHOLARSHIP

- **Best Poster Paper Award in the 24th Korean Conference on Semiconductors** Feb. 2017
(Title : Separate extraction of source and drain resistances in vertically integrated junctionless nanowire field effect transistors, co-author)
- **2016 IEEE Electron Device Society Ph.D. Student Fellowship** Dec. 2016
- **Best Researcher Award for Top-Ranked Achievements in Global Ph.D Fellowship by National Research Foundation (NRF)** (Research Field: Electrical Engineering) Jan. 2016
- **The 22nd HumanTech Paper Award Sponsored by Samsung Electronics - Bronze Prize**
(Title : True fabric-like memory toward wearable electronics, 1st author) Jan. 2016
- **Best Poster Paper Award in the 2015 IEEE Nano** Aug. 2015
(Title : An optimization strategy for low voltage operation of the mechanical switch, co-author)
- **Grand Prize (Kim, Choong-Ki Scholarship) for Top 1 student among the Ph.D. students in School of Electrical Engineering (KAIST)** Apr. 2015
- **Global Ph.D Fellowship Sponsored by National Research Foundation** (3years/\$80,000)
(Individual Project: Investigation of fabrication and characterization based on analysis of interface traps and physical mechanisms in 3D devices) Mar. 2014-Feb. 2017
- **Distinguished Paper in the 2013 Society for Information Display (SID)** May 2013
(Title : Separate extraction technique of intrinsic donor- and acceptor-like density-of-states over full-energy range sub-bandgap in amorphous oxide semiconductor thin film transistors by using one-shot monochromatic photonic capacitance-voltage characteristic, 1st author)
- **SK Hynix Semiconductor Paper Prize in 17th Korean Conference on Semiconductors** Feb. 2010
(Title : Accurate extraction of gate capacitance in leaky MOS systems using modified 3-element circuit model combining the multi-frequency capacitance-voltage method, co-author)
- **Excellence Achievement Award (Graduate Magna Cum Laude)** Aug. 2011
from Graduate School of Kookmin University
- **Scholarship for Graduate Students in Kookmin University (4 Semesters)** 2009– 2011
- **Fellowship for Graduate Students in Kookmin University** Spring 2011
- **Full Four-Year Scholarship for Undergraduate Students in Kookmin University** 2003– 2006

RESEARCH EXPERIENCES

- **Research Assistant : Undergraduate Research Project (URP)** in KAIST (6 months/\$ 4,400)
(Title : Fabrication and improved characterization analysis of physical parameters of TMDC (Transition Metal DiChalcogenides: MoS₂) transistor Jul. 2016–Dec. 2016
- **Research Intensification Course in Global Ph.D Fellowship by NRF** (\$ 4,400)
(NASA Ames Research Center, Moffett Field, California) Feb. 2016
- **Research Project** : Global Ph.D. Fellowship Program Sponsored by NRF Mar. 2014–Feb. 2017
- **Teaching Assistant** : Semiconductor Memory Devices and SoC Design Sep. 2014–Dec. 2014
- **Teaching Assistant** : Course Design for Kit of Wireless Communications using LED Mar. 2014–Aug. 2014
- **Teaching Assistant** : Semiconductor Engineering Mar. 2014–Jun. 2014
- **Industrial-University Cooperation Research** with Samsung Electronics
(Title : DRAM memory based on vertical Ge biristor with gateless and capacitorless structure) 2014– 2017
- **Researcher** Industrial-University Cooperation Research with Samsung Mobile Display
(Title : Modeling & Characterization Techniques for Implementation of Robust LTPS TFTs and Link to Circuit & TCAD Simulators) 2012– 2013
- **Researcher** Industrial-University Cooperation Research with LG Display
(Title : Development of characterization techniques for subgap density-of-states in oxide thin-film transistors with process condition) 2011– 2013
- **National Research Foundation** 2009– 2012
- **Educational Coursework for Semiconductor Device Fabrication Process (the first grade)**
- Inter-University Semiconductor Research Center, Seoul National University, Seoul, Korea Aug. 2009

RESEARCH INTEREST

- Electronic-Textile based Logic-in-Memory toward Wearable Electronics
- 2D Material (MoS₂ & graphene) FET –Fabrication & Electrical Characterization
- Transient Electronics with Dissoluble Substrate based on Printing Technique
- Ge based Vertical Biristor for Gateless 1T-DRAM
- Investigation of Reliability and Instability of Amorphous Oxide Semiconductor (a-IGZO) Thin-Film Transistors and Low-Temperature Poly Silicon Thin-Film Transistors
- Investigation of Physical Mechanism of Organic/Inorganic Material based Resistive Switching Memory
- Device Fabrication and Modeling/Characterization for Si/SiGe MOSFET and 3D Nano-CMOS
- Low-Frequency Noise Characterization
- Opto-Electronic Characterization of Defects in AlGaIn/GaN HEMTs

ACTIVITY

- **IEEE Student Member** (*Electron Device Society*) 2016~
- Golden List of Reviewers of *IEEE Transactions on Electron Devices* 2016, 2015, 2013
- Golden List of Reviewers of *IEEE Electron Device Letters* 2016, 2013, 2012
- Reviewer of *IEEE Electron Device Letter* 2012 ~
- Reviewer of *IEEE Transactions on Electron Devices* 2012 ~
- Reviewer of *AIP Advances* 2016 ~
- Reviewer of *Appl. Phys. Lett.* 2016 ~
- Reviewer of *Journal of Appl. Phys.* 2016 ~
- Reviewer of *Journal of Semiconductor Technology and Science* 2015 ~

MILITARY SERVICE

- **Commissioned Officer** in Electronic Communication through **R.O.T.C.**, Korean Military
- First Lieutenant Mar. 2007–Jun. 2009

PUBLICATIONS

- **Hagyoul Bae**[†], Byung Chul Jang[†] (co-1st author), Hongkeun Park, Soo-Ho Jung, Hye Moon Lee, Jun-Young Park, Seung-Bae Jeon, Gyeongho Son, Kyoungsik Yu, Sung-Gap Im, Sung-Yool Choi^{*}, and Yang-Kyu Choi^{*}, “Functional circuitry on fabric for fibertronics,” *Nature Communications* (Under review).
- **Hagyoul Bae**, Choong-Ki Kim, and Yang-Kyu Choi, “Characterization of intrinsic subgap density-of-states using a multi-frequency conductance-conductance characteristics in exfoliated MoS₂ FETs,” *AIP Advances* (Accepted).
- Jun-Young Park, Byung-Hyun Lee, Geon-Beom Lee, **Hagyoul Bae**, and Yang-Kyu Choi, “Investigation on localized dopant redistribution under ultra-low power of electrothermal annealing from top-down approach,” *Nature Communications*. (Under review).
- Myung-Su Kim[†], **Hagyoul Bae**[†] (co-1st author), Dongil Lee, Byeong-Woon Hwang, Dae-Chul Ahn, Seung-Bae Jeon, and Yang-Kyu Choi, “Characterization of intrinsic field-effect mobility by de-embedding parasitic resistance in graphene field-effect transistors,” *IEEE Journal of Electron Device Society* (Under review).
- Geon-Beom Lee, Choong-Ki Kim, Jun-Young Park, Tewook Bang, **Hagyoul Bae**, Seong-Yeon Kim, Seong-Wan Ryu, and Yang-Kyu Choi, “A novel technique for curing hot-carrier-induced damage by utilizing the forward current of the PN-junction in a MOSFET,” *IEEE Electron Device Letter* (Accepted).
- Seung-Wook Lee, Tewook Bang, Choong-Ki Kim, Kyu-Man Hwang, Byung Chul Jang, Dong-Il Moon, **Hagyoul Bae**, Myungsoo Seo, Seong-Yeon Kim, Do-Hyun Kim, Sung-Yool Choi, and Yang-Kyu Choi, “Comprehensive study on the relation between low-frequency noise and asymmetric parasitic resistances in a vertical pillar-type FET,” *IEEE Electron Device Letter* (Accepted).
- Jun-Young Park, Byung-Hyun Lee, Ki Soo Chang, Dong Uk Kim, Chanbae Jeong, Choong-Ki Kim, **Hagyoul Bae**, and Yang-Kyu Choi, “Investigation of self-heating effects in gate-all-around MOSFETs with vertically stacked multiple silicon nanowire channels,” *IEEE Trans. on Electron Devices* (Under review).
- Gun-Hee Kim, **Hagyoul Bae**, Jae Hur, Choong-Ki Kim, Geon-Bum Lee, Tewook Bang, Yoon-Ik Son, Seong-Wan Ryu, and Yang-Kyu Choi, “Highly biased linear condition method for separately extracting of source and drain resistance in MOSFETs,” *IEEE Trans. on Electron Devices* (Under review).
- Seyeob Kim, **Hagyoul Bae**, Choong-Ki Kim, Myung Keun Lee, Kyung Cheol Choi, and Yang-Kyu Choi, “A Charge density integral method for effective mobility extraction in a-IGZO TFTs by considering the non-uniform distribution of channel charge,” *IEEE Electron Device Letters* (Under review).
- **Hagyoul Bae**[†], Jae-Won Kim[†] (co-1st author), Ogyun Seok, Min Koo Han, Dae Hwan Kim, and Dong Myong Kim, “Opto-electronic characterization of interface traps in AlGaN/GaN HEMTs combining sub-bandgap photons and differential ideality factors,” *IEEE Electron Device Letter* (Under review).
- **Hagyoul Bae**, Tewook Bang, Choong-Ki Kim, Jae Hur, Se-Yeob Kim, Chang-hoon Jeon, Jun-Young Park, Dae-Chul Ahn, Gun-Hee Kim, Yun-Ik Son, Jae-Hoon Lee, Yong-Taik Kim, and Yang-Kyu Choi, “Improved technique for effective mobility by considering gate bias-dependent inversion charges in floating-body Si/SiGe pMOSFET,” *Journal of Nanoscience and Nanotechnology*, vol. 17, no. 5, pp. 3245-3250, May 2017.
- **Hagyoul Bae**[†], Byung-Hyun Lee[†] (co-1st author), Dongil-II Lee, Myeong-Lok Seol, Daewon Kim, Jin-Woo Han, Choong-Ki Kim, Seung-Bae Jeon, Daechul Ahn, Sang-Jae Park, Jun-Young Park, and Yang-Kyu Choi, “Physically transient memory on a rapidly dissoluble paper for security application,” *Scientific Reports*, vol. 6, 38324, Dec. 2016.
- Byung-Hyun Lee[†], Dong-Il Lee[†] (co-1st author), **Hagyoul Bae**, Hyejeong Seong, Seung-Bae Jeon, Myung-Lok Seol, Jin-Woo Han, Meyya Meyyappan, Sung-Gap Im, and Yang-Kyu Choi, “Foldable and disposable memory on paper,” *Scientific Reports*, vol. 6, 38389, Dec. 2016.
- Choong-Ki Kim[†], Eun Gyo Jeong[†] (co-1st author), Eungtaek Kim, Jeong-Gyu Song, Young Jun Kim, Whang Je Woo, Myung Keun Lee, **Hagyoul Bae**, Seung-Bae Jeon, Hyungjun Kim, Kyung Cheol Choi^{*}, and Yang-Kyu Choi^{*}, “Highly stable 2D material (2DM) field-effect-transistors (FETs) with wafer-scale multi-dyad encapsulation,” *IOP Nanotechnology* (Accepted).
- Byung-Hyun Lee, Dae-Chul Ahn, Min-Ho Kang, Seung-Bae Jeon, Tewook Bang, **Hagyoul Bae**, Jun-Young

- Park, Dae-Won Hong, Nam-Soo Park, and Yang-Kyu Choi, “Vertically integrated ZRAM toward extremely scaled memory,” *ECS Transactions*, vol. 75, no. 5, 311-316, Aug. 2016.
- Jun-Young Park, **Hagyoul Bae**, Dong-Il Moon, Chang-Hoon Jeon, and Yang-Kyu Choi, “Threshold voltage tuning technique in gate-all-around MOSFETs by utilizing gate electrode with potential distribution,” *IEEE Electron Device Letters*, vol. 37, no. 11, pp. 1391–1394, Sep. 2016.
 - Dong-Il Lee[†], Jinsu Yoon, Juhee Lee, Byung-Hyun Lee, Myeong-Lok Seol, **Hagyoul Bae**, Seung-Bae Jeon, Hyejeong Seong, Sung-Gap Im, Sung-Jin Choi*, and Yang-Kyu Choi*, “Logic circuits composed of flexible carbon nanotube thin-film transistor and ultra-thin polymer gate dielectric,” *Scientific Reports*, vol. 6, 26121, May 2016.
 - Jun-Young Park, Dong-Il Moon, **Hagyoul Bae**, Young Tak Roh, Myeong-Lok Seol, Byung-Hyun Lee, Hee-Chul Lee, and Yang-Kyu Choi, “Local electro-thermal annealing for repair of total ionizing dose induced damage in gate-all-around MOSFETs,” *IEEE Electron Device Letter*, vol. 37, no. 7, pp. 843–846, Jul. 2016.
 - Chang-Hoon Jeon, Jun-Young Park, Myeong-Lok Seol, Dong-Il Moon, Jae Hur, **Hagyoul Bae**, Seung-Bae Jeon, and Yang-Kyu Choi, “Joule heating to enhance the performance of a gate-all-around silicon nanowire transistor,” *IEEE Trans. on Electron Devices*, vol. 63, no. 6, pp. 2288–2292, Apr. 2016.
 - Ui-Sik Jeong[†], Choong-Ki Kim[†] (co-1st author), **Hagyoul Bae**, Doon-Il Moon, Ji-Min Choi, and Yang-Kyu Choi, “Investigation of low-frequency noise in nonvolatile memory composed of a gate-all-around junctionless nanowire FET,” *IEEE Trans. on Electron Devices*, vol. 63, no. 5, pp. 2210–2213, Mar. 2016.
 - Choong-Ki Kim, Eungtaek Kim, Myung Keun Lee, Jun-Young Park, Myeong-Lok Seol, **Hagyoul Bae**, Tewook Bang, Seung-Bae Jeon, Sang-Hee Park, Kyung Cheol Choi*, and Yang-Kyu Choi*, “An electro-thermal annealing (ETA) method to enhance the electrical performance of amorphous-oxide-semiconductor (AOS) thin-film transistors (TFTs),” *ACS Appl. Mater. Inter.*, vol. 8, no. 36, pp. 23820–23826, Aug. 2016.
 - Choong-Ki Kim[†], Tewook Bang[†], **Hagyoul Bae**, Chang-hoon Jeon, Byung-Woon Hwang, Yun-Ik Son, Jae-Hoon Lee, Yong-Taik Kim, and Yang-Kyu Choi, “Immunity of p-channel Si_{0.8}Ge_{0.2} MOSFET against temperature variation,” *IEEE Electron Device Letter* (Under review).
 - **Hagyoul Bae**[†], Choong-Ki Kim[†] (co-1st author), Seung-Bae Jeon, Gwang Hyuk Shin, Eung Taek Kim, Jeong-Gyu Song, Youngjun Kim, Hyungjun Kim, Sung-Yool Choi, Kyung Cheol Choi, and Yang-Kyu Choi, “A separate extraction method for asymmetric source and drain resistances using frequency-dispersive C-V characteristics in exfoliated MoS₂ FET,” *IEEE Electron Device Letter*, vol. 37, no. 2, pp. 231-233, Jan. 2016.
 - Jun-Young Park, Dong-Il Moon, Myeong-Lok, Seol, Choong-Ki Kim, Chang-Hoon Jeon, **Hagyoul Bae**, Tewook Bang, Jee-Yeon Kim, and Yang-Kyu Choi, “Self-curable gate-all-around MOSFETs using Joule-heating-assisted local annealing for recovery of the hot-carrier degradation,” *IEEE Trans. Electron Devices*, vol. 63, no. 3, pp. 910-915, Jan. 2016.
 - Choong-Ki Kim[†], Chan Hak Yu[†] (co-1st author), Jae Hur, **Hagyoul Bae**, Seung-Bae Jeon, Hamin Park, Yong Min Kim, Kyung Cheol Choi, Yang-Kyu Choi*, and Sung-Yool Choi*, “Abnormal electrical characteristics of multi-layered MoS₂ FETs attributed to the bulk traps,” *2D-Materials*, vol. 3, no. 1, p. 015007, Feb. 2016.
 - Byung-Hyun Lee[†], **Hagyoul Bae**[†] (co-1st author), Hyejeong Seong, Dong-Il Lee, Hongkeun Park, Sung-Gap Im, and Yang-Kyu Choi, “Direct observation of carbon filament in water-resistant organic memory,” *ACS Nano*, vol. 9, no. 7, pp. 7306-7313, Jun. 2015.
 - **Hagyoul Bae**, Jae-Ho Shim, Jae Hur, Byung-Hyun Lee, Chang Hoon Jeon, Kyungsik Yu, and Yang-Kyu Choi, “Characterization of the energy distribution of interface traps based on the photo-responsive subthreshold current in a multi-gate FinFET,” *IEEE Trans. on Electron Devices* (Under review).
 - Jun Seok Hwang, **Hagyoul Bae**, Jungmin Lee, Sung-Jin Choi, Dae Hwan Kim, and Dong Myong Kim, “Sub-bandgap photonic capacitance-voltage method for characterization of the interface traps in low-temperature poly-silicon thin-film transistors,” *IEEE Electron Device Letter*, vol. 36, no. 4, pp. 339-341, Apr. 2015.
 - Hyunjun Choi, Jungmin Lee, **Hagyoul Bae**, Sung-Jin Choi, Dae Hwan Kim, and Dong Myong Kim, “Bias-dependent effective channel length for extraction of subgap DOS by capacitance-voltage characteristics in amorphous semiconductor TFTs,” *IEEE Trans. on Electron Devices*, vol. 62, no. 8, pp. 2689-2694, Aug. 2015.

- **Hagyoul Bae**, Hyojoon Seo, Sungwoo Jun, Hyunjun Choi, Jaeyeop Ahn, Jun Seok Hwang, Jungmin Lee, Saeroonter Oh, Jong-Uk Bae, Sung-Jin Choi, Dae Hwan Kim, and Dong Myong Kim, “Fully current-based sub-bandgap optoelectronic differential ideality factor technique and extraction of subgap DOS in Amorphous semiconductor TFTs,” *IEEE Trans. Electron Devices*, vol. 61, no. 10, pp. 3566-3569, Oct. 2014.
- Jungmin Lee, **Hagyoul Bae**, Jun Seok Hwang, Jaeyeop Ahn, Jun Tae Jang, Jinsu Yoon, Sung-Jin Choi, Dae Hwan Kim, and Dong Myong Kim, “Modeling and separate extraction technique for gate bias-dependent parasitic resistances and overlap length in MOSFETs,” *IEEE Trans. Electron Devices*, vol. 62, no. 3, pp. 1063-1067, Mar. 2015.
- Sungwoo Jun, **Hagyoul Bae**, Hyeongjung Kim, Sung-Jin Choi, Dae Hwan Kim, Dong Myong Kim, and Kyung Rok Kim, “Dual-sweep combinational transconductance technique for separate extraction of parasitic resistances in amorphous thin film transistors,” *IEEE Electron Device Letter*, vol. 36, no. 2, pp. 144-146, Feb. 2015.
- **Hagyoul Bae**, Hyunjun Choi, Sungwoo Jun, Chunhyung Jo, Yun Hyeok Kim, Jun Seok Hwang, Jaeyeop Ahn, Saeroonter Oh, Jonguk Bae, Sung-Jin Choi, Dae Hwan Kim, and Dong Myong Kim, “Single scan monochromatic photonic capacitance-voltage technique for extraction of subgap DOS over the bandgap in amorphous semiconductor TFTs,” *IEEE Electron Device Letter*, vol. 34, no. 12, pp. 1524-1526, Dec. 2013.
- Jaewook Lee, Sungwoo Jun, Jaeman Jang, **Hagyoul Bae**, Hyeongjung Kim, Jong Won Chung, Sung-Jin Choi, Dae Hwan Kim, Jiyoul Lee, and Dong Myong Kim, “Fully transfer characteristic-based technique for surface potential and subgap density-of-states in p-channel polymer-based TFTs,” *IEEE Electron Device Letter*, vol. 34, no. 12, pp. 1521-1523, Dec. 2013.
- Chunhyung Jo, Sungwoo Jun, Woojoon Kim, Inseok Hur, **Hagyoul Bae**, Sung-Jin Choi, Dae Hwan Kim, and Dong Myong Kim, “Characterization of density-of-states and parasitic resistance in a-InGaZnO thin film transistors after negative bias stress,” *Applied Physics Letter*, vol. 102, no. 14, pp. 143502-1–143502-5, Apr. 2013.
- **Hagyoul Bae**, Sungwoo Jun, Hyunjun Choi, Chunhyung Jo, Yun Hyeok Kim, Jun Seok Hwang, Jaeyeop Ahn, Sung-Jin Choi, Dae Hwan Kim, and Dong Myong Kim, “Separate extraction technique for intrinsic donor- and acceptor-like density-of-states over full-energy range sub-bandgap in amorphous oxide semiconductor thin film transistors by using one-shot monochromatic photonic capacitance-voltage characteristics,” *SID Symposium Digest of Technical Papers*, vol. 44, no. 1, pp. 1033-1036, Jun. 2013. (**Distinguish Paper**)
- Sungwoo Jun, Chunhyung jo, **Hagyoul Bae**, Hyunjun Choi, Dae Hwan Kim, and Dong Myong Kim, “Unified subthreshold coupling factor technique for surface potential and subgap density-of-states in amorphous thin film transistors,” *IEEE Electron Device Letter*, vol. 34, no. 5, pp. 641-643, May 2013.
- **Hagyoul Bae**, Hyunjun Choi, Saeroonter Oh, Dae Hwan Kim, Jonguk Bae, Jaehyeong Kim, Yun Hyeok Kim, and Dong Myong Kim, “Extraction technique for intrinsic subgap-DOS in a-IGZO TFTs by de-embedding the parasitic capacitance through photonic C-V measurement,” *IEEE Electron Device Letter*, vol. 34, no. 1, pp. 57-59, Jan. 2013.
- Inseok Hur, **Hagyoul Bae**, Woojoon Kim, Jae Hyeong Kim, Hyun Kwang Jeong, Chunhyung Jo, Sungwoo Jun, Yun Hyeok Kim, Dae Hwan Kim, and Dong Myong Kim, “Characterization of intrinsic field effect mobility by de-embedding the effect of parasitic source and drain resistance,” *IEEE Electron Device Letter*, vol. 34, no. 2, pp. 250-252, Feb. 2013.
- **Hagyoul Bae**, Sungwoo Jun, Choon Hyong Jo, Hyunjun Choi, Jaewook Lee, Yun Hyeok Kim, Seonwook Hwang, Hyun Kwang Jeong, Inseok Hur, Woojoon Kim, Daeyoun Yun, Euiyeon Hong, Hyojoon Seo, Dae Hwan Kim, and Dong Myong Kim, “Modified conductance method for extraction of subgap density-of-states in a-IGZO thin-film transistors,” *IEEE Electron Device Letter*, vol. 33, no. 8, pp. 1138-1140, Aug. 2012.
- **Hagyoul Bae**, Inseok Hur, Ja Sun Shin, Daeyoun yun, Euiyoun Hong, Keum-Dong Jung, Mun-Soo Park, Sunwoong Choi, Won Hee Lee, Mihee Uhm, Dae Hwan Kim, Dong Myong Kim, “Hybrid C-V and I-V technique for separate extraction of structure- and bias-dependent parasitic resistances in a-InGaZnO TFTs,” *IEEE Electron Device Letter*, vol. 33, no. 4, pp. 534-536, Apr. 2012.

- Seok Cheon Baek, **Hagyoul Bae**, Dae Hwan Kim, and Dong Myong Kim et al., “Avalanche hot source method for separated extraction of parasitic source and drain resistances in single Metal-Oxide-Semiconductor field effect transistors,” *Journal of Semiconductor Technology and Science*, vol. 12, no. 1, pp. 46-52, Mar. 2012.
- Euiyoun Hong, Daeyoun Yun, **Hagyoul Bae**, Hyunjun Choi, Won Hee Lee, Mihee Uhm, Hyojoon Seo, Jieun Lee, Jaeman Jang, Dae Hwan Kim, and Dong Myong Kim, “Sub-bandgap optical differential body-factor technique and characterization of interface states in SOI MOSFETs,” *IEEE Electron Device Letter*, vol. 33, no. 7, pp. 922-924, Jul. 2012.
- Ja Sun Shin, Hyunjun Choi, **Hagyoul Bae**, Jaeman Jang, Daeyoun Yun, Euiyoun Hong, Dae Hwan Kim, Dong Myong Kim, “Vertical gate Si/SiGe double HBT-based capacitorless 1T DRAM Cell for extended retention time at low latch voltage,” *IEEE Electron Device Letter*, vol. 33, no. 2, pp. 134-136, Feb. 2012.
- Jun-Hyun Park, Yongsik Kim, Sungchul Kim, **Hagyoul Bae**, Dae Hwan Kim, and Dong Myong Kim, “Surface potential-based analytic DC I-V model with effective electron density for amorphous Indium-Gallium-Zinc-Oxide thin film transistors considering parasitic resistances,” *IEEE Electron Device Letter*, vol. 32, no. 11, pp. 1540-1542, Nov. 2011.
- Sunyeong Lee, Ja Sun Shin, Jaeman Jang, **Hagyoul Bae**, Daeyoun Yun, Dae Hwan Kim, and Dong Myong Kim, “A novel capacitorless DRAM Cell using superlattice band-gap engineered(SBE) structure with 30nm channel length,” *IEEE Transactions on Nanotechnology*, vol. 10, no. 5, pp. 1023-1030, Sep. 2011.
- Daeyoun Yun, Minkyung Bae, Jaeman Jang, **Hagyoul Bae**, Ja Sun Shin, Euiyeon Hong, Jieun Lee, Dae Hwan Kim, and Dong Myong Kim, “Differential body-factor technique for characterization of interface traps in MOSFETs,” *IEEE Electron Device Letter*, vol. 32, no. 9, pp. 1206-1208, Sep. 2011.
- Ja Sun Shin, **Hagyoul Bae**, Jaeman Jang, Daeyoun Yun, Jieun Lee, Dae Hwan kim, and Dong Myong Kim, “A narrow bandgap SiGe channel superlattice bandgap engineered (SBE) 1T DRAM cell for low voltage operation and extended hole retention time,” *Semiconductor Science and Technology*, vol. 26, 095025, Aug. 2011.,
- Ja Sun Shin, **Hagyoul Bae**, Jaeman Jang, Daeyoun Yun, Jieun Lee, Euiyoun Hong, Dae Hwan Kim, and Dong Myong Kim, “A novel double HBT-based capacitorless 1T DRAM cell with Si/SiGe heterojunctions,” *IEEE Electron Device Letter*, vol. 32, no. 7, pp. 850-852, Jul. 2011.
- **Hagyoul Bae**, Sungchul Kim, Minkyung Bae, Ja Sun Shin, Dongsik Kong, Hyunkwang Jung, Jaeman Jang, Jieun Lee, Dae Hwan Kim, Dong Myong Kim, “Extraction of separated source and drain resistances in amorphous Indium-Gallium-Zinc-Oxide TFTs through C-V characterization,” *IEEE Electron Device Letter*, vol. 32, no. 6, pp. 761-763, Jun. 2011.
- **Hagyoul Bae**, Jaeman Jang, Ja Sun Shin, Daeyoun Yun, Jieun Lee, Tae Wan Kim, Dae Hwan Kim, and Dong Myong Kim, “Modeling and characterization of separate extraction of gate bias- and channel length-dependent intrinsic and extrinsic source-drain resistances in MOSFETs,” *IEEE Electron Device Letter*, vol. 32, no. 6, pp. 722-724, Jun. 2011.
- Ja Sun Shin, **Hagyoul Bae**, Euiyoun Hong, Jaeman Jang, Daeyoun Yun, Jieun Lee, Dae Hwan Kim, Dong Myong Kim, “Modeling and extraction technique for parasitic resistances in MOSFETs combining DC I-V and low frequency C-V measurement,” *Solid-State Electronics*, vol. 72, pp. 78-81, Jun. 2011.
- **Hagyoul Bae**, Seok Cheon Baek, Sunyeong Lee, Jaeman Jang, Ja Sun Shin, Daeyoun Yun, Hyojong Kim, Dae Hwan Kim, and Dong Myong Kim, “Separate extraction of source, drain, and substrate resistances in MOSFETs with parasitic junction current method,” *IEEE Electron Device Letter*, vol. 31, no. 11, pp. 1190-1192, Nov. 2010.

INTERNATIONAL CONFERENCE

- Myungsoo Seo[†], **Hagyoul Bae**[†] (co 1st author), Do-Hyun Kim, Sung Kwan Lim, Byoung Hun Lee, and Yang-Kyu Choi, “Novel analysis of interface traps and bulk traps of a polycrystalline silicon thin film transistor,” *2017 MRS Fall Meeting, Boston, USA* (Under review).

- Myungsoo Seo[†], **Hagyoul Bae**[†] (co 1st author), Chang-Hoon Jeon, Byung-Hyun Lee, and Yang-Kyu Choi, “Advanced characterization technique for the extraction of intrinsic effective mobility in ultra-thin-body strained SOI MOSFETs,” *IEEE SOI-3D-Subthreshold Microelectronics Unified Conference (S3S)*, San Francisco, USA (Just Accepted).
- Byung-Hyun Lee, Dae. Chul Ahn, M. H. Kang, S.-B. Jeon, T. Bang, **Hagyoul Bae**, J.-Y. Park, D. W. Hong, N. S. Park, and Yang-Kyu Choi, “Vertically integrated Zram (VI-zRAM) toward extremely scaled memory,” *Proceeding of ECS Meeting, Honolulu* (2016).
- Byung-Hyun Lee, Dong-Il Lee, **Hagyoul Bae**, Jae Hur, Dae-Chul Ahn, and Yang-Kyu Choi, “An optimization strategy for low voltage operation of the mechanical switch,” *2015 IEEE Nano (Best paper award)*.
- **Hagyoul Bae**, Sungwoo Jun, Hyunjun Choi, Chunhyung Jo, Yun Hyeok Kim, Dae Hwan Kim, and Dong Myong Kim, “Separate extraction technique of intrinsic donor- and acceptor-like density-of-states over full-energy range sub-bandgap in amorphous oxide semiconductor thin film transistors by using one-shot monochromatic photonic capacitance-voltage characteristics,” *SID Int. Symp. Tech. Dig. Papers*, May 2013 (**Distinguished Paper**).
- Chunhyung Jo, **Hagyoul Bae**, Sungwoo Jun, Hyunjun Choi, Seonwook Hwang, Dae Hwan Kim, Byung-Du Ahn, Je-Hun Lee, and Junho Song, and Dong Myong Kim, “Characterization of asymmetrical negative bias stress effect on the density-of-states and parasitic resistances in a-IGZO thin-film transistors,” *SID Int. Symp. Tech. Dig. Papers*, May 2013.
- Sunyeong Lee, Jaeman Jang, Ja Sun Shin, Hyojong Kim, **Hagyoul Bae**, Daeyoun Yun, Dae Hwan Kim, and Dong Myong Kim, “A Novel Superlattice Band-Gap Engineered (SBE) Capacitorless DRAM cell with extremely short channel length down to 30 nm,” *2010 IEEE International Memory Workshop (IMW)*, pp. 16– 19, May 2010.

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EQUIPMENT and CAD TOOL

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- ICP Asher, Spin Coater, Wet-Station
 - Evaporator, Sputter
 - MA6, MJB4 (Photolithography)
 - Furnace (Oxidation, Annealing)
 - Inkjet Printer (UJ-200 MF)
 - Scanning Probe Microscopy (SPM)
 - Atomic-Force Microscopy (AFM)
 - Scanning Electron Microscope (SEM)
 - Cadence OrCAD (Software Tool)
 - Agilent 4156C / 4145B Semiconductor Parameter Analyze
 - HP 4294A Precision Impedance Analyzer / HP 4284A High Precision LCR Meter
 - HP 35670A Dynamic Signal Analyzer
 - SR 570 Low-Noise Current Amplifier
 - ILX Lightwave FOM-7900B Multi-Channel Fiber Optic Test System (1310nm, 1550nm)
 - OZ 1000 - Fiber Optics Sources (460 nm, 530 nm, 620 nm)
 - MPS-8033 Precision Fiber Optic Sources (850nm)
 - Vacuum Chamber M5VC Cylindrical Probe Station (MST-5000-CHAMBER)
 - MMR Tech.: Low Temperature Micro Probing System
 - Cascade Microtech Microwave Probe Station
 - Silvaco ATLAS Device Simulation Software
 - Synopsys Device Simulation Software

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