Vertically Integrated ZRAM toward Extremely Scaled Memory

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This paper discusses the demonstration of a vertically integrated gate-all-around (GAA) silicon nanowire (SiNW) channel-based dynamic random access memory (DRAM) without a cell-capacitor as a breakthrough for conventional DRAM scaling. Owing to the one-route all-dry etching process (ORADEP) with stiction-free stability and process simplicity, vertical integration of multiple silicon nanowire was achieved with high uniformity and high reproducibility. Finally, high performance suitable for further scaling was presented in zero-capacitor DRAM (ZRAM) operable with up to five-story SiNW channels without sacrificing scalability.

Introduction

With the advance of information and communication technology (ICT), the rapid processing of explosively increasing amounts of data is becoming important. This has led to the need for high-speed memory which operates with low power consumption. Dynamic random access memory (DRAM), which has been a driving force in the growth of the memory market over the past several decades, has used as the main memory based on its high speed at the embedded system level, whereas flash memory has mainly been employed as secondary memory for high-capacity storage. In terms of productivity, the fabrication cost, and performance, DRAM has been advanced given that it has been continuously scaled. Due to the advent of 20nm DRAM, [1] however, it faces a severe impasse in relation to more aggressive miniaturization. In particular, cell capacitor, which is used to store data in DRAM, is the bottleneck. Under this circumstance, an approach to DRAM without cell capacitor, known as one-transistor DRAM (1T-DRAM) or zero-capacitor DRAM (ZRAM), [2] is very timely. As shown in Figure 1, ZRAM has a few strengths compared to conventional DRAM. In addition to reduced chip size and greater process simplicity due to the absence of cell capacitor, [3] sense amplifier (S/A) to identify the data state in DRAM is not needed for ZRAM. Because it provides an opportunity for a versatile style of circuit architecture in what was originally the S/A area, it is feasible for improving the performance of ZRAM beyond the advantage of chip scaling. However, the removal of the S/A demands a high sensing current to identify the data state correctly and quickly, which is crucial to guarantee stable operation of ZRAM.

Another factor impeding the miniaturization of DRAM is the short channel effects (SCEs), [4] which are problematic in electronic devices with embedded metal-oxide-semiconductor field-effect transistors (MOSFETs). It cannot therefore be exceptional in DRAM. To overcome the SCEs, MOSFET has evolved from the conventional two-dimensional (2-D) gated structure to the 3-D gated structure, enabling the prolongation of Moore's law. [5]

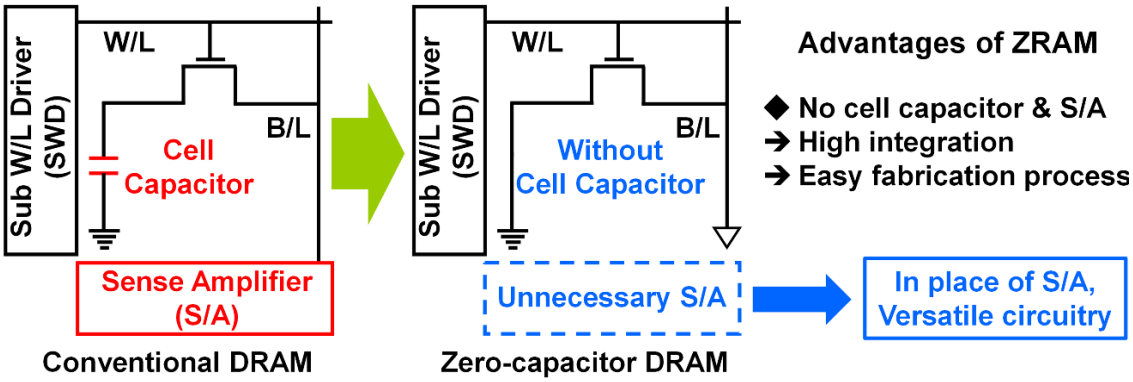

Figure 1. Comparison of conventional DRAM with 1T-1C and ZRAM with only 1T.

Among the various 3-D structures currently available, gate-all-around (GAA) silicon nanowire (SiNW) is reportedly the ultimate configuration for effectively suppressing the SCEs due to its greatly enhanced gate controllability. [6] However, continuous scaling requires a reduction of the SiNW volume; this is beneficial for the suppression of the SCEs due to the enhanced gate controllability but detrimental to the current drivability due to the reduced channel area.[7] In this respect, Lee *et al.* suggested a vertically integrated SiNW FET which utilizes a stiction-free and simple fabrication process, resulting in high performance and the effective suppression of the SCEs without a sacrifice of scalability.[8,9] Accordingly, vertically integrated SiNW-based ZRAM can provide a clue for the continuous scaling of DRAM beyond 20 nm.

In this study, vertically integrated five-story GAA SiNW-based ZRAM is demonstrated. Unlike previous results, [10-12] the one-route all-dry etching process (ORADEP) used here enables the formation of vertically integrated SiNW with high stability and high reproducibility. An image of the fabricated device was clearly identified with the aid of transmission electron microscopy (TEM). The transfer characteristics depending on the number of channels were compared in FET with one- and five-story SiNW. Ultimately, the device demonstrated that an increase in the sensing current crucial for ZRAM operation is feasible with relatively more SiNW, enabling further scaling for another type of DRAM capable of operating at high speeds.

Fabrication

An eight-inch bulk-silicon wafer was used as the substrate in this work. The vertical integration of the SiNW was completed with the aid of the ORADEP. Figure 2(a) shows a schematic of the ORADEP. One cycle in the ORADEP consists of C_4F_8-based polymer passivation followed by a SF_6-based isotropic dry etching process, where iteration of the cycle permits vertical integration of multiple SiNWs. The number of cycles is equal to that of vertically integrated SiNW. Figure 2(b) shows a scanning electron microscopy (SEM) image of a fabricated vertically integrated SiNW. [8,9] A stiction-free and uniform pattern of multi-stacked SiNWs is identified in the image. Thereafter, to isolate the transistors, low-pressure chemical vapor deposition (LPCVD)-based silicon dioxide (SiO_2) was deposited as an inter-layer dielectric (ILD), followed by planarization using a chemical-mechanical polishing (CMP) process. Trench holes were formed for the formation of the embedded gate electrode. SiO_2 as a gate dielectric was then thermally grown on the surface of the SiNW. Poly-Si, which serves as a gate electrode, was deposited, fully surrounding SiNW with gate oxide. It enables a building of the complete GAA structure. The exposed

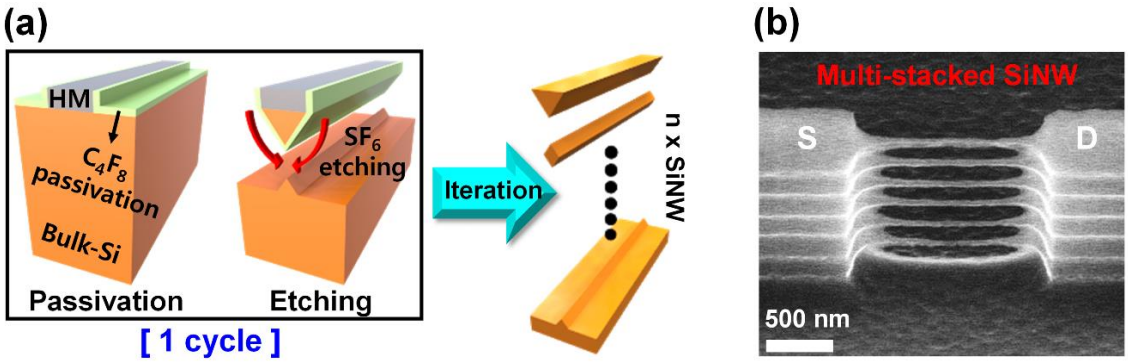

Figure 2. (a) A schematic of the ORADEP. (b) SEM image of the vertically integrated SiNW fabricated by means of the ORADEP.

top gate electrode was patterned using a krypton fluoride (KrF) laser-based photolithography and dry etching process. An implantation step for the formation of source/drain (S/D) electrode was done and was followed by an annealing process to activate the implanted dopants. Finally, the device was completed with forming gas anneal (FGA).

Results and Discussion

A schematic and TEM images of the fabricated device are presented in Figure 3. Figure 3(b) shows the cross-sectional TEM image along the a-a' direction in Figure 3(a). Five vertically integrated SiNWs are uniformly formed without stiction failure, owing to the use of the optimized ORADEP. For reference, no wet etching process and sequential dehydrating process is used in the ORADEP. Figure 3(c) shows an enlarged image of the SiNW in Figure 3(b). Thermally grown SiO_2 surrounds the rhombus-type SiNW, and poly-Si that wraps this realizes the complete GAA configuration.

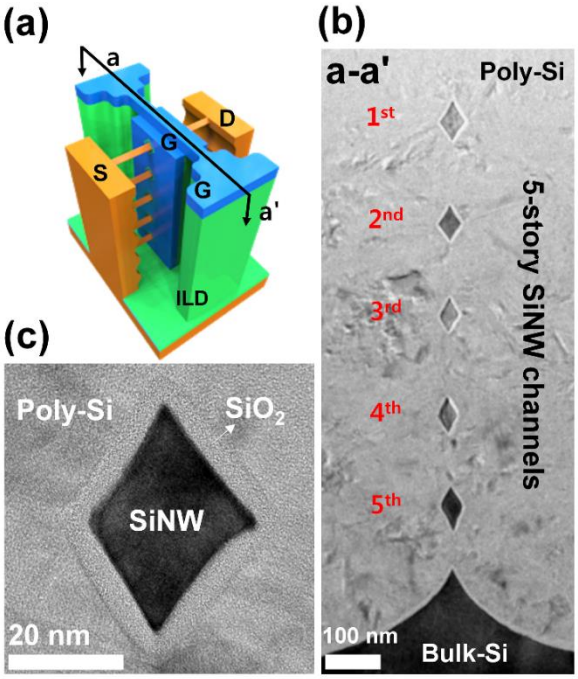

Figure 3. (a) A schematic of the fabricated device. (b) TEM image of the fabricated device. (c) Enlarged image of the SiNW in Figure 3(b).

Figure 4(a) exhibits the transfer characteristics, *i.e.*, the drain current (I_D)-gate voltage (V_G) characteristics, showing a comparison of these characteristic between a FET with a one-story SiNW channel and a FET with a five-story SiNW channel. The FET with the five-story SiNW presents improved current drivability compared to that of the FET with the one-story SiNW. No significant degradation of the crucial transistor parameters was noted during the enhanced performance, which supports the reliability of the fabrication process including the ORADEP. In Figure 4(b), the increase of I_D is summarized as a function of V_G, which clearly shows the remarkably improved performance capability.

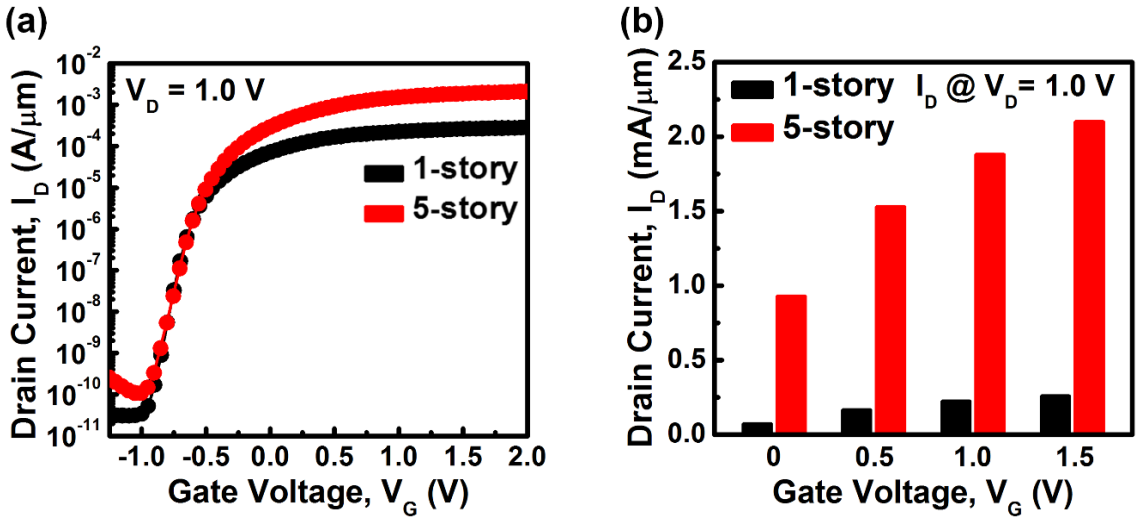

Figure 4. (a) I_D-V_G characteristic of the FET with the one-story SiNW channel and the five-story SiNW channel. (b) Comparison of I_D as a function of the selected V_G.

Figure 5(a) exhibits the ZRAM operation of the five-story SiNW FET via the I_D-V_G characteristic. As shown in Figure 5(a), the FET shows typical I_D-V_G characteristic as a switching device when the V_D value is low, *e.g.*, 1 V. However, I_D rapidly increases at a high V_D value of around 5 V, showing a very steep subthreshold slope (SS) below 10 mV/dec. Such a low SS below 60 mV/dec is challenging to achieve in a thermionic emission-operated FET. This abrupt increase of I_D is due to impact ionization, a fundamental mechanism of ZRAM operation. As an electron moves from the source to the drain, hot electrons with high levels of energy due to an electric field generate electron-hole pairs via confliction to another electron. The generated holes then accumulate in the SiNW body and consequently activate a parasitic bipolar junction transistor (BJT) in the form of the n^+ (source)-p (body)-n^+ (drain). The parasitic BJT serves as another driving source, thereby maintaining a high current even when the gate electrode is an off state. This phenomenon is known as single transistor latch (STL) behavior, [13] giving rise to a rapid increase in the current with a steep SS. As a result, during forward and reverse sweeps of V_G, the hysteresis curve shown in Figure 5(a) results from the positive feedback mechanism due to the STL-triggered parasitic BJT operation. The operation characteristics of the ZRAM with one- and five-story SiNW are compared in Figure 5(b). During the forward sweep of V_G, unlike the subthreshold state (1), each ZRAM shows a rapid increase of I_D at approximately the threshold voltage (2), where V_D to trigger the STL behavior is applied. Owing to the activated parasitic BJT, each ZRAM can retain a high level of current during the reverse sweep of V_G (3), even under a subthreshold state. However, the five-story SiNW

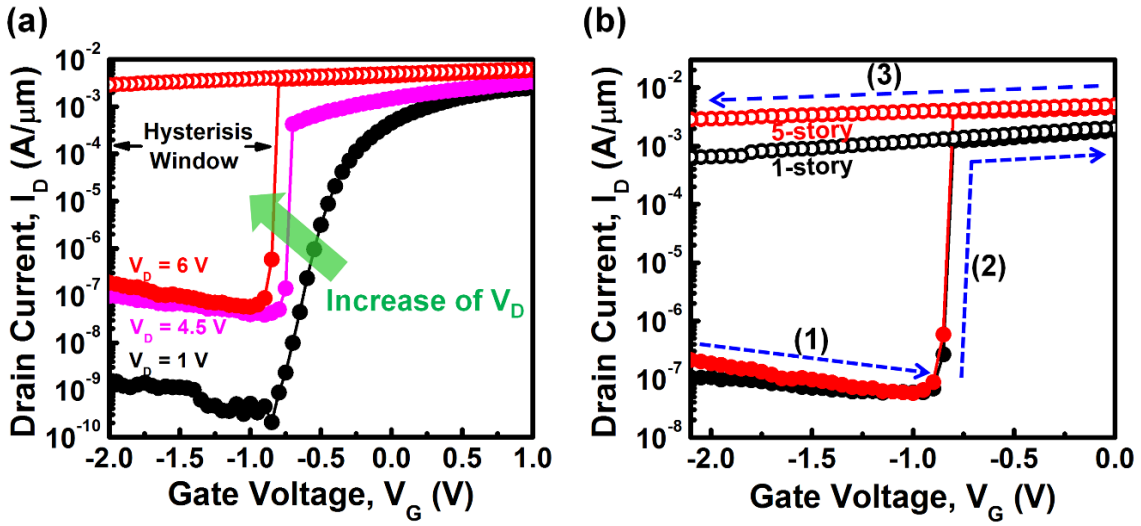

Figure 5. (a) ZRAM operation with a hysteresis loop during positive and negative bias sweeps. (b) Comparison of the ZRAM operation between ZRAM with a one-story SiNW channel and that with a five-story SiNW channel. Compared to the one-story SiNW ZRAM, an increased sensing memory window is identified in the five-story SiNW ZRAM.

ZRAM shows a larger current than that of the one-story SiNW ZRAM, corresponding to the results shown in Figure 4. Accordingly, the vertically integrated five-story SiNW channel-based ZRAM exhibits a larger sensing current at particular reading voltage, *e.g.*, -1 V, resulting in an increase of the memory window to identify the data state compared to the one-story SiNW ZRAM. Considering the absence of the S/A in the ZRAM, this result is very desirable in view of stable data sensing. It enables a reduction of the chip size and provides an opportunity for versatile forms of circuit architecture as the occasion demands.

Conclusions

In summary, ZRAM with vertically integrated GAA SiNWs was developed to demonstrate the feasibility of extremely scaled DRAM, where the optimized ORADEP supported the integrity of the fabricated device. The five-story ZRAM exhibited a remarkably improved sensing current window corresponding to the number of integrated SiNW channels. In terms of scalability, this result maximizes the strength of ZRAM, which does not need a capacitor or, even an S/A. The results here will help to realize the ultimate scaling of DRAM toward its roadmap end.

Acknowledgments

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