Experimental study on Quantum Mechanical Effect for Insensitivity of Threshold Voltage against Temperature Variation in Strained SOI MOSFETs

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The temperature dependence of threshold voltage (V_T) in a thin-body MOSFET, which was built on a strained silicon-on-insulator (sSOI) wafer, is examined in a temperature range of 173 K to 373 K. The insensitive temperature dependency of threshold voltage (V_T) is attributed to the strain effect arisen from the sSOI, which makes the energy quantization stronger due to the lowered conductivity mass. Additionally, enhanced mobility of 770 cm^2/V•sec at room temperature is achieved due to the strain effect.

Keywords— silicon on insulator (SOI), strained SOI (sSOI), quantum mechanical effect, temperature dependency, threshold voltage, ultra-thin body (UTB).

I. INTRODUCTION

The strained devices built on a ultra-thin body (UTB), utilizing the best of both worlds, are considered as a leading solution for future technology [1]. Although there were many precedent studies of conventional non-strained UTB device such as interplay between carrier transport and quantum confinement as UTB thickness becomes thinner [2-4], there is no enough study on interaction between the strain and quantum confinement, which may alter the band structure in a nanoscale body.

This work focused on temperature dependency on the electrical properties of strained SOI FinFETs such as threshold voltage and mobility with consideration of both the strain and quantum confinement effect. It is found that the strain on UTB enhances the quantum mechanical effect from the fact that the threshold voltage (V_T) is barely sensitive to the temperature variation.

II. EXPERIMENTAL DETAIL

A strained n-channel FinFET was fabricated on a strained silicon on insulator (sSOI) wafer with a channel thickness (T_{Si}) of 10 nm and (100) surface orientation. The starting material was an undoped sSOI wafer consisting of T_{Si} of 15 nm. Afterwards, it was thinned down to 10 nm by sacrificial oxidation and subsequent removal of the oxide. The sSOI wafer has 1.3 G-Pascal biaxial tensile strain with a buried oxide thickness (T_{BOX}) of 145 nm (SOITEC). Fins were patterned by simple Si mesa etching. The gate stack consists of gate oxide of 2.7 nm formed by dry oxidation and in-situ phosphorus doped poly-crystalline Si (poly-Si). Fig.1 (a) and (b) show high-resolution transmission electron microscopy (TEM) images of a 16 nm gate length and of a 10 nm fin height (T_{Si}=H_{Fin}). Arsenic implantation for the source and drain electrodes was done subsequent to the formation of the gate spacer. Dopant activation was carried out for 5 s at 1000 ^{o}C. Metallization processes consisted of inter-layer dielectric deposition, contact etching, tungsten deposition, and patterning with conventional CMOS technology.

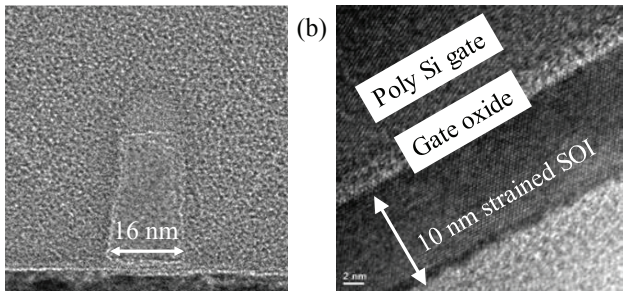

Fig. 1. High-resolution cross-sectional TEM images. (a) 16-nm gate length, (b) 10-nm channel thickness

For mobility extraction depending on the gate voltage, a large sized FinFET (L=50 μm and W=50 μm) was utilized to obtain current-voltage (*I-V*) and capacitance-voltage (*C-V*) characteristics. For low-temperature measurements between 173 K and 300 K, a cryogenic probe station with liquid nitrogen at a pressure of 1 mTorr was used. Thereafter, the effective mobility was extracted by means of the split *C-V* method using the measured I-V and *C-V* characteristics. Also V_T was characterized in a range of 173 K to 300 K.

III. ELECTRICAL CHARACTERIZATION

Fig. 2 (a) shows a typical transfer characteristic for the case with forming gas annealing (FGA) versus that without the FGA. The FinFET applied with FGA showed an ideal subthreshold swing of 60 mV/dec, whereas that without FGA shows a degraded subthreshold swing of 80 mV/dec owing to the insufficient passivation of the interface. Fig. 2 (b) also shows that the low field mobility is drastically enhanced from 480 cm^2/Vs to 770 cm^2/Vs via the FGA process. From the plot of the mobility versus inversion charge density

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shown in Fig. 2 (b), the influence of coulomb scattering on the low field mobility was clearly suppressed due to the passivation effect of FGA. As a consequence, the obtained mobility value in this work is comparable to that reported in other previous works. And it is obvious that the strain influences on electron transports in the UTB as expected.

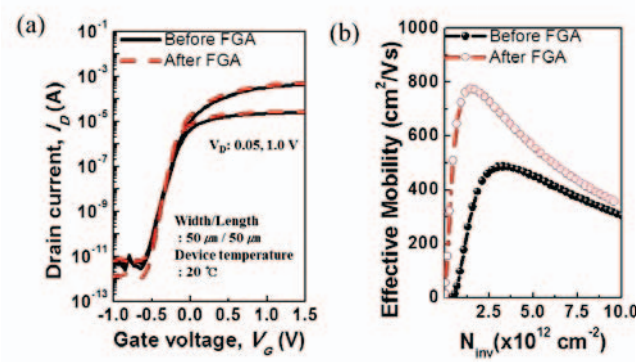

Fig. 2. Comparison of (a) the transfer curve and (b) the effective mobility before and after the FGA process. The effective mobility was extracted from measured data by the split C-V method

Transfer curves at a low drain bias are shown in Fig. 3 (a) at various temperatures. Fig. 3 (b) is a close-up view of Fig. 3 (a), showing that V_T, which was extracted by the linear extrapolation method, tends to be lower due to the drain current decrement by temperature increment.

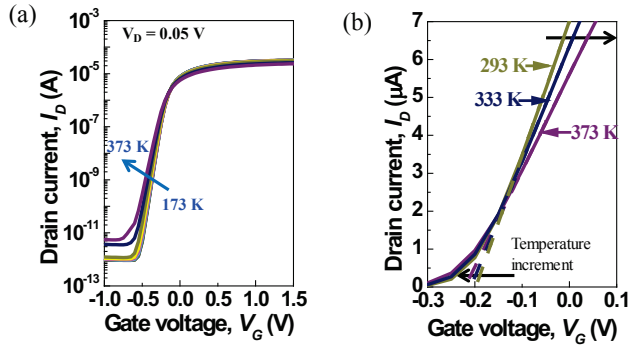

Fig. 3. (a) Transfer curve in a temperature range of 173 K to 373 K, and (b) close-up view of (a) converted to a linear-linear plot

The extracted electron mobility levels versus the inversion charge densities for various temperatures are shown in Fig 4 (a). For convenience' sake, a temperature range is broken into two parts: the region I from 173 K to 250 K and the region II from 250K to 373K. The low field mobility is nearly identical in the region I. And the observed representative peak mobility at 250 K exceeds 860 $cm^2/V{\cdot}sec$. As the temperature surpasses 250 K, the mobility starts to decrease due to enhanced phonon scattering in the region II. This is consistent with the decrease of the saturation drain current above 250 K shown in Fig 4. (b). On the other hand, V_T also starts to decrease as the temperature surpasses 250 K. In detail, V_T is barely changed in the region I and it is slightly decreased in the region II. This is attributed to drain current decrement due to the abovementioned boosted phonon scattering.

The temperature dependence of V_T in fully depleted (FD) SOI MOSFETs has been described extensively [4-7]. The V_T variation with the temperature in the FD SOI MOSFETs is notably smaller than that in bulk MOSFETs because it is primarily caused by the variation of the depletion depth. Recently, it was found that when the thickness of the silicon channel is less than 5 nm, the V_T variation according to the temperature tends to be reduced further due to the quantum confinement effect [4]. Medury *et al.* showed that V_T was insensitive to the temperature variation due to the strengthened quantum effect when the SOI thickness was thinned enough. Especially, the quantization effect became stronger compared to temperature related effects when the thickness of the silicon channel without the strain effect was less than 3 nm [4]. As shown In Fig. 4 (b), although V_T starts to slightly decrease in the region II where the phonon scattering dominantly governs the drain current decrement, V_T is nearly invariant in the region I. In this work, even though the body thickness is 10 nm, which is thicker than the thickness (≤3 nm) of other non–strained UTB devices [4, 5], the invariance of V_T against temperature variation is also found. This is primarily attributed to intensified quantum effect aided by the strain effect. Electrons in the two-fold valleys of (100) surface have lowered conductivity mass and it is anticipated that the energy levels in the strained SOI layer can be strongly quantized even at a relatively thick SOI thickness.

As a consequence, the strengthened quantum mechanical effect should be considered when the device is designed with the strained UTB structure. Leaving the mobility enhancement aside, the temperature dependence of V_T is also a critical concern for the strained UTB, which is influenced by co-effect of the strain and quantum confinement effect.

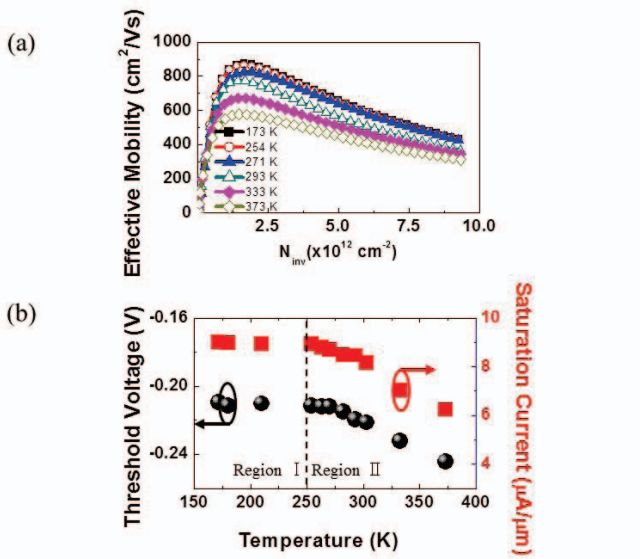

Fig. 4. (a) Temperature dependence of the effective mobility, and (b) temperature dependence of the threshold voltage and the saturated drain current. The threshold voltage was determined from the *x*-intercept point, which was projected from the linearly extrapolated line on the maximum g_m point. The saturated drain current was read at gate and drain voltage of 1.0 V

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IV. CONCLUSIONS

The electrical characteristics of the strained FinFET fabricated on the strained SOI (sSOI) wafer were evaluated in a temperature range of 173 K to 373 K. V_T was barely changed below the temperature of 250 K where the phonon scattering started to make an impact on the mobility. From the insensitive behavior of V_T to temperature variation, the strain effect from the sSOI makes the energy quantization stronger. These physical understandings should be considered in designing devices with the strained ultra-thin body structure such as a multi-gate FET.

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