Flexible High-performance Nonvolatile Memory by Transferring GAA Silicon Nanowire SONOS onto a Plastic Substrate

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Abstract

Flexible nonvolatile memory is demonstrated with excellent memory properties comparable to the traditional wafer-based rigid type of memory. This achievement is realized through the transfer of an ultrathin film consisting of single crystalline silicon nanowire (SiNW) gate-all-around (GAA) SONOS memory devices onto a plastic substrate from a host silicon wafer.

Introduction

Flexible electronics [1-5] are one of the most promising future technologies. Enabled by their flexibility, their advantages over traditional semiconductor devices on rigid substrates support their widespread application. Organic semiconductors [1,5] are typically utilized for low-cost applications despite their poor device performance and low density, while inorganic semiconductors [2-4] have recently been considered for high-performance flexible devices. Meanwhile, flexible types of memory [5,6] have been developed for fully functional flexible systems. However, the flexible memory devices reported thus far have large feature sizes with poor performance compared to conventional silicon wafer-based types of memory. This situation is caused by material limitations and the limited fabrication methods feasible for use with plastic substrates, such as high-temperature manufacturing processes and processes requiring highly sophisticated equipment. In this paper, we show, for the first time, flexible high-performance inorganic memory transistors that perform excellent memory properties with highly scaled-down dimensions similar to those of traditional wafer-based rigid memory devices.

Fabrication of the Flexible GAA SONOS FETs

The photographs shown in **Fig.1** are of GAA SONOS FETs on a SOI wafer (Fig. 1a), and these devices after being transferred onto a plastic substrate (Fig. 1b). The transferring sequence from a SOI wafer to flexible polyimide tape is schematically illustrated in **Fig. 2**. The process begins with coating a protection layer on the GAA SONOS devices, followed by attachment to a temporary handler. Afterwards, the silicon handle layer underneath the buried oxide (BOX) layer is chemically etched out until the BOX layer is exposed, where the BOX acts as an etch stop layer of Si. A 5% tetramethyl ammonium hydroxide solution at 90°C is used for the Si etching. The remaining ultrathin film layer consisting of the GAA SONOS devices is approximately 1 μm thick. Finally, the ultrathin film is transferred onto a flexible film with a thickness of 35 μm, followed by the removal of the temporary handler and the protection layer. **Fig. 3** depicts the details of the fabrication process used to create GAA SONOS FETs on a wafer [7] and associated TEM images. The starting wafer was a SOI wafer with a top silicon thickness of 110 nm. The top silicon was thinned down to 50 nm by sequential oxidation and wet etching processes. The top silicon layer was patterned to form a SiNW with 50 nm width. The width of the SiNW was further reduced to 30 nm by sacrificial oxidation and removal process. The Si NW was then suspended by wet etching the BOX underneath the SiNW with diluted HF solution. The large size source/drain probe pads served as the anchors, physically supporting the suspended SiNW. Afterwards, the charge trapping trilayer structure was sequentially formed with O/N/O layers having thicknesses of 3/7/12 nm, respectively. A n+ in-situ poly-Si layer was then deposited, and poly-Si/O/N/O layers were patterned simultaneously. The S/D was formed by implantation and activation processes. Then, a PECVD silicon dioxide layer was deposited and the via holes were patterned. Finally, aluminium was deposited and then patterned to form the metal pads for the probing.

Results and Discussions

All electrical characterizations of the GAA SONOS FETs were done with a gate length of 100 nm and a SiNW width and height of 30 nm each. **Fig. 4** shows a comparison of the transfer and output characteristics of the GAA SONOS FETs before and after the transfer process. The stability of the process during transferring steps is confirmed, since no device degradation is observed. **Fig. 5** shows the results of bending analysis of the fabricated flexible devices under different bending conditions. Mechanical stability is also confirmed by the negligible difference in performance when the flexible substrate is bent. The high-performance electrical characteristics of the fabricated flexible devices arise from the traditional CMOS fabrication processes utilized, and the excellent gate controllability due to the GAA structure despite the thick gate dielectric.

As with the preceding typical transistor characterizations, all characterizations of memory functionalities were carried out with GAA SONOS FETs under three different conditions: (i) with the initial devices fabricated on a SOI wafer, (ii) after the devices are transferred onto the flexible substrate, and (iii) with the flexible devices in a bent condition with a bending radius of 1 cm (corresponding to a strain of 0.1%, smaller than the strain at the fracture strength as shown in **Fig. 12b**). Program and erase operations are carried out by the FN tunneling mechanism.

Typical I_D-V_G hysteresis curves of the GAA SONOS for various program and erase voltages (V_{PGM}, V_{ERS}) are shown in **Fig. 6** and **Fig. 7**, respectively. Duration of the program and erase times (t_{PGM}, t_{ERS}) are 10 ms, and 100 ms, respectively. Acceptable NVM characteristics are achieved with the aid of O/N/O dielectric stacks as the charge storage node. A V_T window of about 4 V is achieved with a V_{PGM} value of 14 V and a V_{ERS} value of -14 V. **Fig. 8** and **Fig. 9** show the detailed program and erase transient behaviors, respectively. Moreover, the nonvolatile-memory (NVM) transient characteristics of the GAA SONOS are retained after the devices are transferred onto the polyimide from the host silicon wafer, and even under the bent condition.

To analyze the reliability of the NVM, typical values of V_{PGM} = 14 V, t_{PGM} = 10 ms, V_{ERS} = -14 V, t_{ERS} = 100 ms are used. A V_T window of more than 2.5 V is sustained for retention behavior longer than 10 years, as shown in **Fig. 10**. Endurance characteristics exceeding 10^4 program/erase cycles are obtained as well, as shown in **Fig. 11**. It should be noted that the NVM reliability is also maintained after the GAA SONOS devices were transferred onto the polyimide from the host silicon wafer, and even under the bent condition.

The present flexible NVM performance levels show not only the best performance among all flexible memory types to the best of our knowledge, but they also satisfy the traditional technical specifications of commercialized NVM. Moreover, there is no doubt that current commercially available products with extremely scaled-down devices can be turned into flexible products by adopting the presented transferring techniques.

The influence of plastic thickness on mechanical stability was analytically investigated, as shown in **Fig. 12**. The strain suffered by the devices varies according to the thickness of the flexible substrate. This supports that the optimization of the total film thickness can move ultra-flexible electronics with improved practicality toward realization. A film design in which the devices lie near the neutral mechanical plane would be the best option for the ultra-flexibility.

Conclusions

High-performance GAA SONOS nonvolatile memory was demonstrated on a flexible substrate through a transfer process, and its reliability was confirmed by a bending test. The proposed flexible nonvolatile memory has nanoscale dimensions, and shows the best nonvolatile memory performance to date on flexible substrates. Moreover, this device also satisfies the technical specifications of commercialized non-flexible nonvolatile memory.

References

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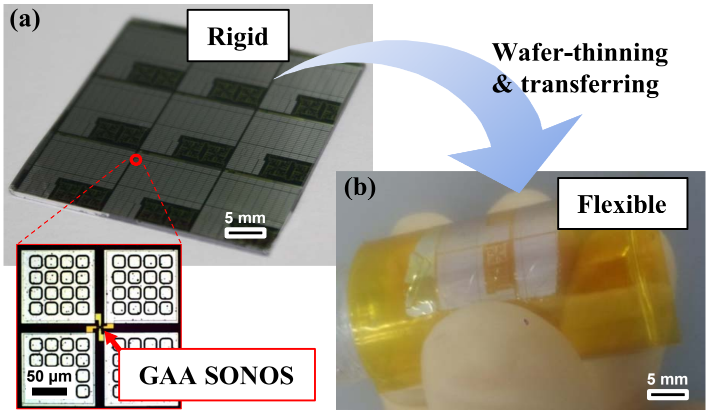


Fig. 1 (a) Photograph of the as-fabricated GAA SONOS FETs on a SOI wafer. **(b)** Photograph of the ultrathin GAA SONOS devices transferred onto a flexible substrate.

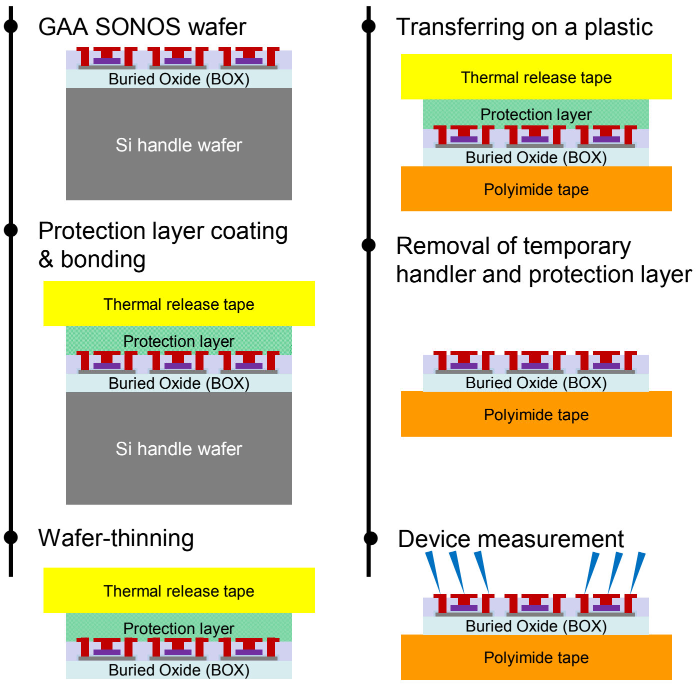


Fig. 2 Schematic illustration of the wafer thinning procedures and subsequent steps for transferring the high performance GAA SONOS onto a flexible substrate.

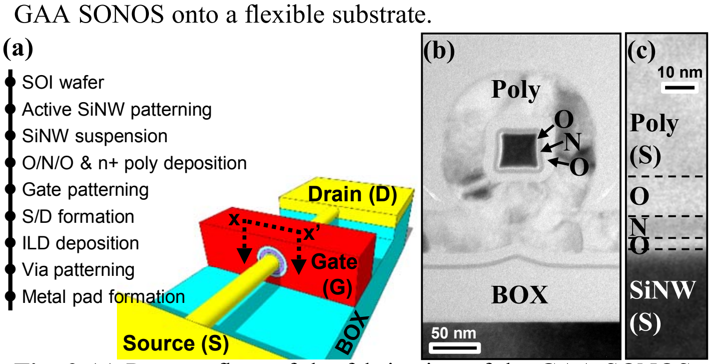


Fig. 3 (a) Process flow of the fabrication of the GAA SONOS and a 3-D schematic diagram of the GAA SONOS before ILD deposition. **(b)** A TEM image of the GAA SONOS along the x-x' direction of Fig. 3(a). **(c)** A TEM image of O/N/O (3/6/13 nm) layers for the nonvolatile memory operation.

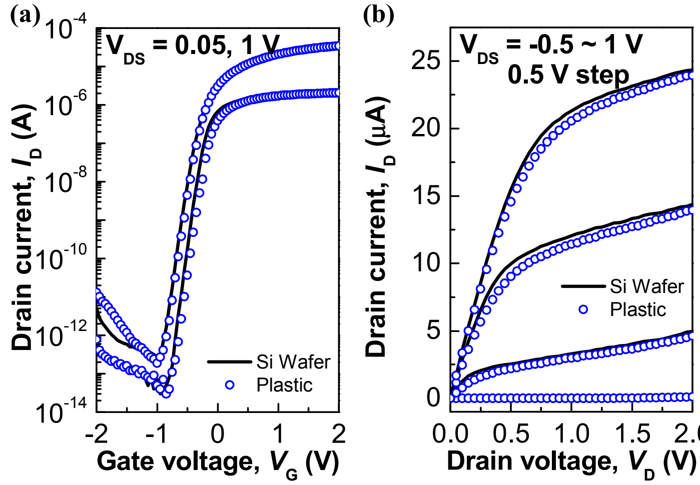


Fig. 4 Representative **(a)** Transfer and **(b)** Output characteristics of the GAA SONOS devices, before and after the ultrathin film transferring process. The changes in the I_D-V_G and I_D-V_D characteristics are negligible, proving the stability of the wafer-thinning and transfer processes.

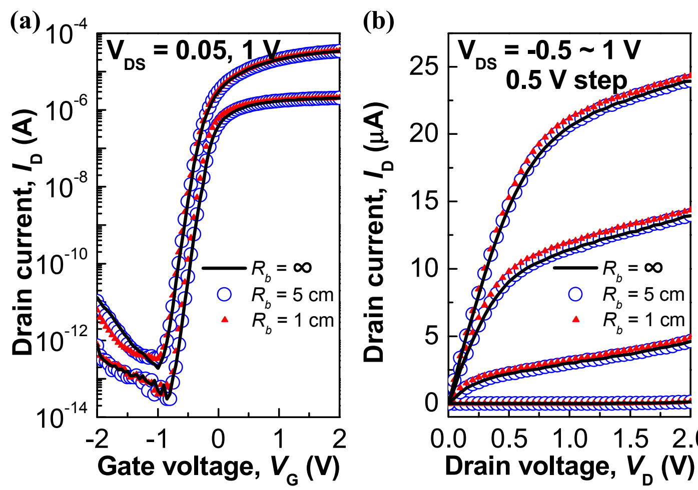


Fig. 5 (a) Transfer and **(b)** Output characteristics of the flexible GAA SONOS devices under different bending conditions. Mechanical stability is confirmed that nearly unchanged device characteristics are shown.

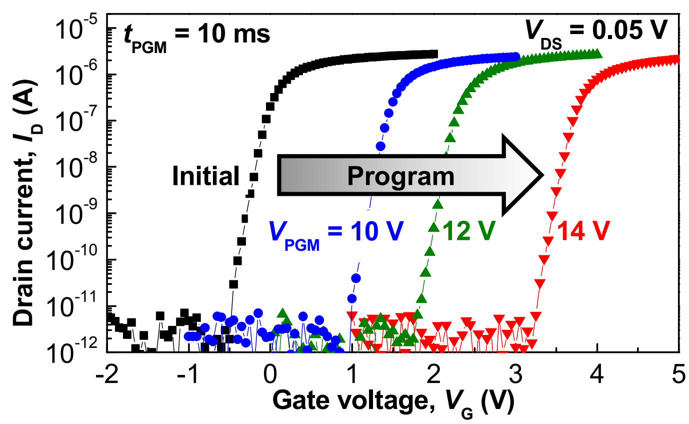


Fig. 6 Typical program characteristics. I_D-V_G curves with various program voltage (V_{PGM}) on the GAA SONOS device.

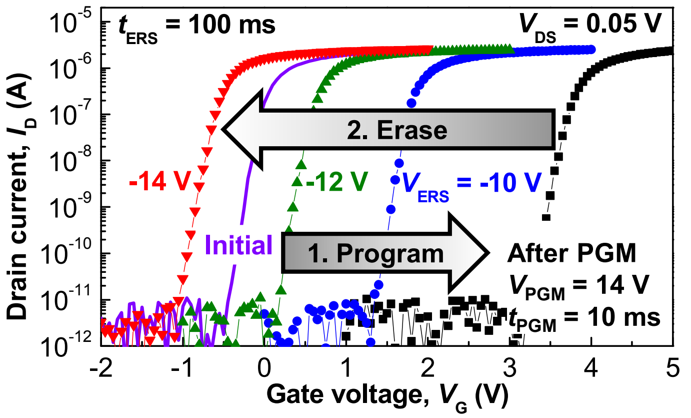


Fig. 7 Typical erase characteristics. I_D-V_G curves with various erase voltage (V_{ERS}) on the GAA SONOS device.

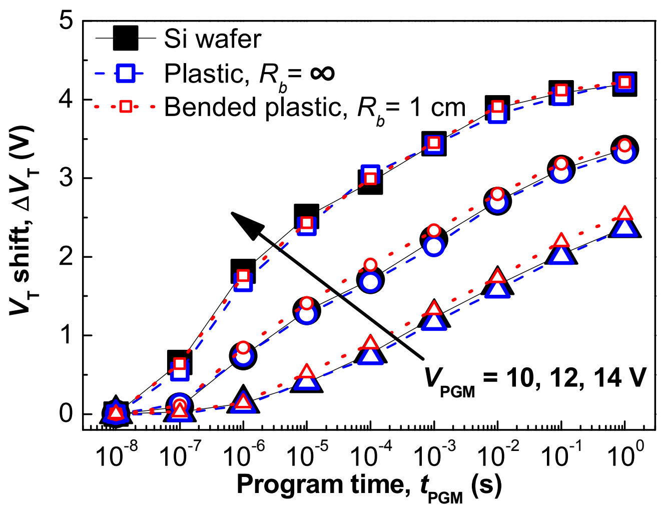


Fig. 8 Speed response of programming for nonvolatile memory operation with various V_{PGM} conditions. Program transient characteristics of the GAA SONOS is preserved after the devices are transferred onto a plastic, and even under bending.

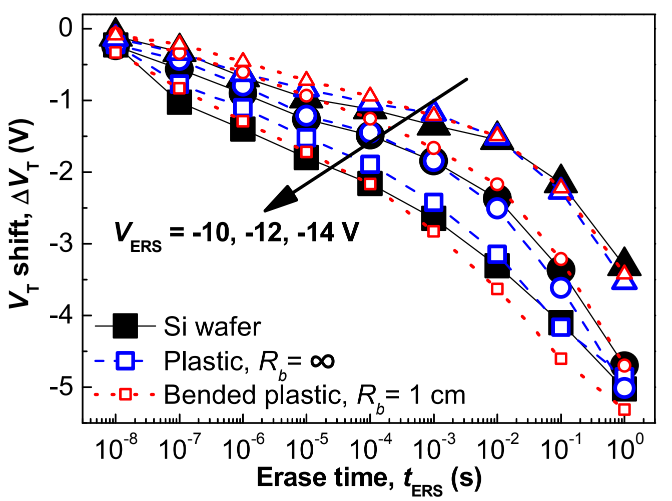


Fig. 9 Speed response of erasing for nonvolatile memory operation with various V_{ERS} conditions. Erase transient characteristics of the GAA SONOS is preserved after the devices are transferred onto a plastic, and even under bending.

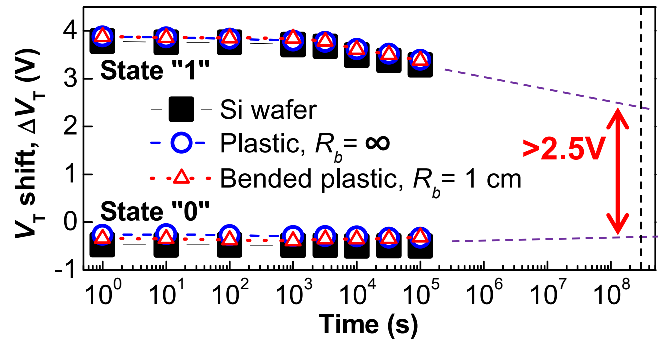


Fig. 10 Retention characteristics of the GAA SONOS. 10 years of retention is guaranteed with V_T window of more than 2.5 V. Retention characteristic of GAA SONOS is preserved after the devices are transferred onto a plastic, and even under bending.

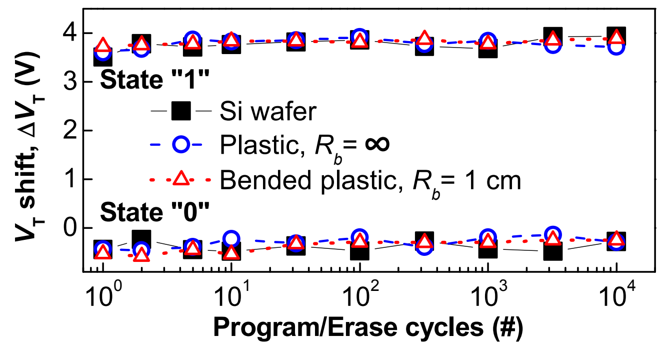
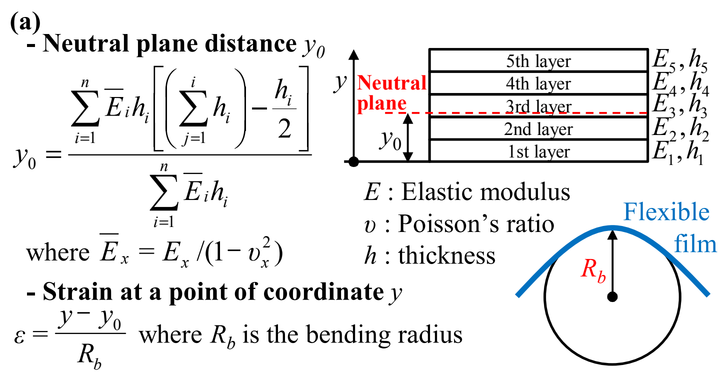
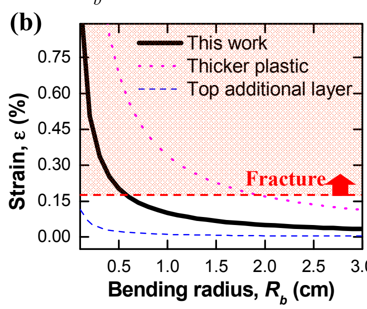


Fig. 11 Endurance characteristics of the GAA SONOS. The V_T window is maintained after 10^4 P/E cycles. Endurance characteristic of GAA SONOS is preserved after the devices are transferred onto a plastic, and even under bending.





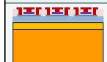
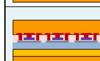
Case	Plastic thickness
	35 μm (This work)
	75 μm (Thicker plastic)
	35 μm + 25 μm (Top additional layer)

Fig. 12 (a) Simple modeling of the strain under bending. **(b)** The strain suffered by the devices versus bending radius (R_b). Mechanical endurance can be controlled by the film thickness engineering of the substrate.