Nanogap Electrode Fabrication for a Nanoscale Device by Volume-Expanding Electrochemical Synthesis

Ju-Hyun Kim, Hanul Moon, Seunghyup Yoo, and Yang-Kyu Choi*

A novel nanogap fabrication method using an electrochemical nanopatterning technique is presented. Electrochemical deposition of platinum ions reduces the microgap size to the sub-50-nm range due to the self-limited volume expansion of the electrodes. Additionally, the low crystallinity of platinum reduces the line edge roughness in the electrodes, whereas the high crystallinity of gold increases it. Current compliance, a buffered resistor, and a symmetric deposition strategy are used to achieve high reliability and practicality of nanogap electrodes. As a possible application, an organic thin-film transistor using the nanogap electrodes is also demonstrated.

1. Introduction

Nanogap electrodes have received a considerable amount of attention as a means of integrating nanometer-sized molecules into macroscopic electronic devices, as nano-electronic devices have developed rapidly with the aid of nanofabrication technology.[1] Several fabrication techniques for nanogap electrodes have been reported and are widely used in the field of nanodevices. Direct writing techniques such as e-beam lithography and dip-pen lithography can produce nanometer-scale patterns but are inevitably time-consuming processes.[2–6] Thus, they cannot be used for mass-production. Electromigration and breakdown techniques provide simple and fast fabrication methods for nanogap electrodes.[7–13] However, limited size control issues with these techniques represent a critical disadvantage. Alternatively, there are other novel fabrication techniques, such as those based on a molecular ruler,[14–16] chemical deposition,[17,18] tilted-angle shadow evaporation,[19–21] and on the focused ion beam (FIB) method.[22–24] Although numerous nanogap fabrication methods have been reported, it remains challenging to manufacture controllable and reliable nanogap electrodes in large numbers. In most cases, accurately controlled methods often require long processing times, whereas high-throughput techniques are associated with a lack of controllability and reliability.

To overcome the aforementioned problems, the electrochemical (EC) method combined with conductance feedback and a self-limited scheme was introduced.[25–32] In these methods, metal microgap electrodes are prepared using conventional optical lithography or e-beam lithography, and the EC deposition of metal ions enlarges the initial electrodes, resulting in the reduction of the gap size. As the gap size decreases, the conductance between the two electrodes increases and a feedback system automatically terminates the further EC deposition at a certain level of conductance. These techniques provide a rapid manufacturing speed and reliable controllability; however, the deposited metal ions often produce a rough surface due to their intrinsic crystallinity, especially in the case of gold, which has often been employed in the EC deposition method.[17,29] This phenomenon tends to increase the line-edge roughness of the nanogap electrodes significantly, and it can have adverse effects on devices with nanogap electrodes (see Figure S1 in Supporting Information for details). Therefore, controlling the crystallinity of the EC-deposited material, if possible, has significant implications but also imposes a technical challenge.

2. Results and Discussion

In this study, we introduce a fabrication method for a platinum nanogap electrode based on EC deposition and
self-limited termination by a current compliance system with the aid of a parameter analyzer to achieve a smooth nanogap surface. The method improves the uniformity and repeatability of the gap size by preventing the crystallization of the electrochemically deposited metal ions. When the voltage is applied across the reference and working electrode, platinum ions start to become deposited onto the pre-patterned Pt electrodes without crystallization. Hence, a smooth nanogap of sub-50 nm is fabricated with a reliably controlled geometrical structure. A buffered external resistor method and a symmetric deposition method for producing nanogap electrodes are used to enhance the practicality and stability of these devices to promote a wider range of applications. Finally, pentacene nanogap organic thin-film transistors (OTFTs) were fabricated to demonstrate the feasibility of the proposed platinum-based nanogap electrodes. A schematic of the fabrication method used to create the self-limited platinum nanogap electrodes is illustrated in Figure 1. Conventional lithography, platinum metal deposition, and a lift-off process were used for the fabrication of the microgap. Afterwards, electrochemical synthesis of platinum was done to expand the size of the electrodes and reduce the initial gap size to the sub-50-nm range (see Experimental Section and Figure S2 in Supporting Information for details).

It should be noted that voltage optimization in EC deposition is crucial because the voltage level is the most important factor when attempting to ensure smooth electrode surfaces. The corresponding results are summarized in Figure 2. The electrochemical reduction mechanism of the metal ions can be explained in terms of the electron supply, initial nucleation and positioning (settlement), and the growth of the metal nuclei (volume expansion). As the voltage is applied between the working and reference electrodes, the working electrode starts to provide electrons to platinum ions near the electrode surface thereafter the platinum ions are reduced to platinum metal, resulting in the creation of the initial nuclei. Afterwards, the nuclei settle down on the working electrode surface and induce the volume expansion of the electrode by the continuous reduction of platinum ions near the nuclei. In order to make the stable reduction of gold ions on the working electrode surface and avoid a scattered cluster formation for the smooth volume expansion, sufficient time should be applied for the nuclei to settle down on the working electrode surface. If the reduction speed is too fast, due to excessively high voltage and a rapid electron supplying rate, the initial nuclei will be grown onto clusters before settling down on the electrode surface. This results in an in-solution reduction. The starting voltage was 2.5 V, and the Pt ions began to cluster and aggregate in the solution. This phenomenon can be explained by the significantly fast reduction of the Pt ions. It is important to note that an excessively high voltage induces a violent reaction of Pt ions. As a result, the ions cannot stabilize the reaction on the electrode surface. Randomly scattered reductions occur, even in the solution, and violently produce many clusters on the electrodes. Consequently, surface reduction for stable volume expansion is comparatively inhibited in the working electrodes. Figure 2a shows the results of the EC deposition at 2.0 V. Although the size of the Pt clusters decreased, the gap region was still

![Figure 1](image-url)  
**Figure 1.** A schematic of the nanogap fabrication steps using electrochemical (EC) deposition. a) The highly doped Si substrate acts as a back-gate for OTFT application, and a patterned low-pressure chemical vapor deposition tetraethyl orthosilicate (LPCVD TEOS) layer is fabricated for device-to-device isolation. b) Thermal oxide is grown for a gate oxide and isolation between two microgap electrodes. c) A Pt microgap is fabricated by optical lithography, metal deposition, and a lift-off process. d) Pt EC deposition causes a volume expansion of the microgap electrodes and reduces the gap size to the nanometer scale.
covered with aggregated clusters. This result is similar to that under the 2.5 V condition.

At a voltage of 1.6 V, however, the situation changed dramatically and most of the Pt ion reduction occurred on the surface of the working electrode (Figure 2b). Under this optimized condition, there was neither cluster formation nor in-solution reduction. Thus, the Pt ions had sufficient time to reach the electrode surface and stabilize the electrochemical reaction via Pt atom-to-atom deposition. As a result, controllable volume expansion of the working electrodes was achieved and the size of the microgap was gradually reduced to the nanogap range. In other words, a lower voltage level is favorable for creating fewer clusters and for a smoother volume expansion. However, there is the requirement of a minimum voltage level to trigger the electrochemical reaction for ion reduction. When the voltage is less than 1.5 V, according to our research, the electrochemical deposition rate is too low to accomplish both a volume expansion and a nanogap reduction. Figure S3a–c show respective SEM images of a platinum microgap after electrochemical deposition at 1.5, 1.3, and 1.1 V for 809 s, which is same deposition time used during the deposition at 1.6 V shown in Figure 2b. The result shows that the volume expansion of the working electrode at 1.5 V successfully reduced the nanogap, whereas the volume expansion trials at 1.3 and 1.1 V were unsatisfactory due to the slow deposition speed. According to these results, we concluded that the 1.6 V condition is the optimized voltage condition for a smooth volume expansion of the electrode, with additional voltage of 0.1 V for reliable and robust electrochemical deposition.

The unique characteristics of various applied voltages were also analyzed from the measured current data. A comparison of the real-time read current for clusters with serious line-edge roughness and volume expansion without line-edge roughness is shown in Figure 2c. In the case of clustering at a supply voltage of $V_s = 2.0$ V, there were only three minor peaks without a major peak that reached the compliance level. At this point, the working and reference electrodes were connected instantaneously by the in-solution-generated clusters, as shown in Figure 2a. These clusters either floated in the solution or were unstably attached to the electrode. Therefore, the connections through these clusters could not be sustained for a long period. As a result, the two electrodes became disconnected after a short time due to breakdown. This, in turn, caused the current to decrease to the baseline level. The localized connections between the clusters continuously formed during EC deposition and again produced minor peaks. As a result, there was no stable volume expansion of the working electrodes, and EC deposition was not completed according to current compliance specifications. In contrast, there was only one major peak in the final stage for volume expansion without clustering at $V_s = 1.6$ V. The absence of intermediate minor peaks indicated that the EC deposition was automatically complete at a current compliance of 50 μA and a synthesis time of 809 s. A simple and distinctive read current profile was attained by the stable volume expansion of the working electrode. This also indicates that there were no Pt clusters between the two electrodes to trigger the rapid increase and decrease of the current level during the EC deposition process, as shown in Figure 2b.

To improve the stability of the nanogap formation process, we studied and compared two types of EC deposition strategies. Typically, Pt ions are deposited on only one side, that is, the working electrode (see the Supporting Information, Figure S4a). In this case, a difference in height between the two electrodes, i.e., the working and reference electrodes, was inevitable due to the asymmetric volume expansion at the working electrode. The gap size was reduced from one side of the working electrode to produce a thick Pt layer, whereas nothing transpired at the reference electrode. This asymmetric structure has no advantage in terms of stability and practicality. This drawback arising from the asymmetric structure can be circumvented by switching the bias polarity iteratively. Because the Pt ions were reduced and deposited on the electrode under negative bias during EC deposition, this iterative switching of the bias polarity induces a symmetric volume expansion at both the working and reference electrode (see the Supporting Information, Figure S4b). This simple and useful strategy for symmetric deposition can enhance both the reliability and stability of nanogap electrodes and the
practicality of their broad application. Figure 3a shows the real-time read current of the symmetric nanogap synthesis under alternating switching of the bias polarity between the two electrodes. The EC deposition voltage was 1.6 V, and the deposition time for 1 cycle was 60 s. For each cycle, the polarity of the synthesis voltage was switched for symmetric volume expansion between both electrodes; in addition, the current polarity was also changed according to bias polarity switching. During the 6th deposition cycle, the measured current increased rapidly and showed a major peak, signifying that the nanogap fabrication process was complete.

Additionally, we introduced one additional electrical setup, which was to employ an external resistor for reliable nanogap fabrication. When the formation of the nanogap was completed by sufficient volume expansion of the microgap electrodes, the major peak current was monitored in the parameter analyzer and the voltage supply was automatically stopped by current compliance, as shown in Figure 2c. Due to the greater rapid increase of the major peak current with respect to the sampling rate of the parameter analyzer (10 Hz in this work), however, the nanogap electrode could be exposed to a high current over the compliance level for 0.1 s in the worst case. This current overshoot produces high mechanical stress in the nanogap electrodes and can partially damage them. Figure 3b shows a damaged electrode due to the current overshoot. Here, a part of the electrode is lifted off from the substrate. The damaged electrode is not only mechanically and electrically unstable but also cannot likely be used for further applications. To overcome this problem, an external resistor was connected in series between the parameter analyzer and the probe tip. The external resistor is a passive element, which allows it to respond to an abrupt increase in current and act as a voltage divider; thus, the resistor provides damage protection for the well-defined nanogap electrodes. In this work, a 100-kΩ external resistor was used to avoid overshoot damage, and I_{sat}, the saturation current, was 18.1 μA during the final stage of nanogap formation. With the aid of the external buffer resistor during EC deposition, the nanogap electrodes can reproduce a stable and reliable structure, as shown in Figure 3c. SEM images of the fabricated nanogap electrode using the combinational method of the EC deposition, symmetrical and cyclic biasing, and an external resistance buffer are shown in Figure 4. The EC deposition was successfully carried out without any clusters, and both electrodes were symmetrically expanded up to sub-50 nm (approximately 46 nm) in terms of the gap size without overshoot damage with the aid of the optimized bias condition, the cyclic bias scheme, and the external resistor.
setup. In this case, the initial microgap size was 1 μm and fabricated nanogap size was 46 nm. The total electrochemical deposition time to the saturation of current was 311 s as shown in Figure 3a (1 cycle is 60 s and the process is finished at 11 s of sixth cycle). As a result, the growth velocity of electrodes was 3.1 nm/s.

The electrical characteristics of the EC-deposited nanogap were verified by fabricating an OTFT and measuring its I–V characteristics. Figure 5 shows the $I_D$–$V_G$ and $I_D$–$V_D$ characteristics of the microgap OTFT and nanogap OTFT. A 50-nm thick pentacene film serving as the hole-transporting organic material was deposited as a channel layer on the fabricated microgap and nanogap devices by vacuum sublimation. The channel width was 10 μm for both devices. As a long channel device, the microgap OTFT had a channel length (corresponding to the gap size) of 10 μm. Gate modulation and drain current saturation were observed as typical characteristics of a field-effect transistor (Figure 5a). As a short channel device, the nanogap OTFT had a channel length of sub-50 nm, as shown in Figure 4b. In this case, gate modulation was also observed, but the drain current was not saturated (Figure 5c). This characteristic is similar to that noted in conventional short-channel MOSFETs. It is caused by drain-induced barrier lowering (DIBL) and the punch-through effect, as the space-charge-limited current (SCLC) prevents saturation of the drain current and because SCLC increases as the drain voltage increases.

The EC-deposited nanogap OTFT showed the results expected for a short-channel OTFT when compared to those of a microgap OTFT. In addition, we calculated the threshold voltage and the mobility of fabricated OTFT. The threshold voltage $V_T$ was extracted by maximum $g_m$ method by differentiating $I_D$–$V_G$ curve shown in Figure 5b,d, where $g_m$ is the transconductance defined by $g_m \equiv \partial I_D / \partial V_G$. As a result, the threshold voltage of a microgap OTFT ($V_{TM}$) was −1.35 V and that of a nanogap OTFT ($V_{TN}$) was −2.1 V. At the threshold voltage, the transconductance of the microgap OTFT ($g_{mM}$) was 3.9 nS and that of the nanogap OTFT ($g_{mN}$) was 16.6 nS. The mobility $\mu$ is defined as

$$\mu = \frac{g_m L}{C_V V_D W}$$

where $C_V$, $L$, and $W$ are the gate capacitance (per unit area), a channel length, and a channel width, respectively. In this work, 15-nm-thick thermal silicon dioxide was used as gate oxide and the drain voltage was 1 V. The channel length of the microgap OTFT ($L_M$) was 10 μm and that of the nanogap OTFT ($L_N$) was 46 nm. The channel width was 50 μm for all OTFTs. From the listed parameters and Equation (1), we calculated the mobility at the threshold voltage. The mobility of the microgap OTFT ($\mu_M$) was 2.26 cm$^2$ V$^{-1}$ s$^{-1}$ and that of the nanogap OTFT ($\mu_N$) was 0.044 cm$^2$ V$^{-1}$ s$^{-1}$. The mobility value
3. Conclusion

In summary, we demonstrated a Pt nanogap fabrication method using EC deposition and real-time current monitoring with the aid of a parameter analyzer. The low crystallinity of Pt led to the reliable formation of a smooth and uniform nanogap with the help of voltage optimization. In addition, a symmetrical cyclic bias scheme and external buffer resistor were introduced for a practical and reliable nanogap structure. As a possible application, short-channel organic thin-film transistors were successively fabricated with pentacene active layers formed on the microgap and nanogap template. This proposed nanogap fabrication method can be extended to various applications, such as single molecule detection, chemical and biomolecule sensing, and the fabrication of next-generation field-effect transistors and memory devices due to its simple, fast, and reliable characteristics, which are compatible with large-scale fabrication and mass-production processes.

4. Experimental Section

The micro/nanogap structures used in our study were fabricated by a combinational method combining a conventional semiconductor fabrication technique and electrochemical synthesis. As a starting substrate, a 4-inch silicon wafer was heavily doped by phosphorous implantation with 80 keV of energy and a dose of $5 \times 10^{15} \text{ cm}^{-2}$ to form a conductive layer (back-gate). To minimize the leakage current between the back-gate and nanogap electrodes, tetraethyl orthosilicate (TEOS) oxide at a thickness of 500 nm was deposited, and 30 $\mu$m $\times$ 30 $\mu$m square patterns for active areas were defined by optical lithography and HF wet etching. Subsequently, a 15-nm-thick gate oxide was grown in the active areas by dry thermal oxidation at 900 °C for 10 min. Additional lithography was carried out to delineate the photoresist patterns for an initial microgap. A 10-nm layer of chrome and a 100-nm layer of platinum were sequentially deposited on the patterned photoresist. The patterned photoresists were then lift-off with metals deposited on the unwanted regions. These metal electrodes with micropip sizes served as the working and reference electrodes for the subsequent EC deposition. The designed initial gap size (distance between two electrodes) ranged from 1 to 10 $\mu$m.

After the fabrication of the microgap, a polydimethylsiloxane (PDMS) well was attached to the center of the microgap array chip to contain the Pt ion solution for EC deposition. For preparation of the Pt ion solution, chloroplatinic acid ($\text{H}_2\text{PtCl}_6$) (10 mw) and poly-vinylpyrrolidone (PVP) (20 g/L) were mixed as the ion source and surfactant, respectively. The Pt ion solution was introduced into the PDMS well, and extended pads of the microgap electrodes were connected to an Agilent 4156C, the parameter analyzer, with the aid of a probe station. The parameter analyzer supplied voltage between both electrodes for EC deposition and simultaneously read the current level between them. As the deposition advanced with the electrochemical reduction of Pt ions, the read current increased due to the expansion of the electrodes and the reduction of the gap size. The power supply from the parameter analyzer was terminated when the read current exceeded the value of the current compliance, and the fabrication of the nanogap electrodes thus finished automatically (see Figure S2 in Supporting Information).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MEST) (No. 2009-0083079).


Received: November 23, 2010
Revised: January 17, 2011
Published online: