A Novel Junctionless All-Around-Gate SONOS Device with a Quantum Nanowire on a Bulk Substrate for 3D Stack NAND Flash Memory

Sung-Jin Choi, Dong-Il Moon, J. P. Duarte, Sungho Kim, and Yang-Kyu Choi
EE, KAIST, Daejeon, Korea
Email: ykchoi@ee.kaist.ac.kr, Phone: +82-42-350-3477, Fax: +82-42-350-8565

ABSTRACT

A novel junctionless all-around-gate (AAG) SONOS device with a homogeneously n^+-doped silicon nanowire (SiNW) is demonstrated on a bulk substrate. The diameter and gate length of the quantum-scale SiNW are 4 nm and 20 nm, respectively. A deep RIE process is developed for the formation of the SiNWs. The junctionless AAG SONOS device shows a high read current (> 10 μA), a large V_T margin (> 6.5 V), a narrowed distribution of the erased V_T, and improved cyclic endurance (10^5 cycles). Moreover, the proposed process is applied to implement vertically integrated 9-layer single-crystal SiNWs for 3D NAND.

INTRODUCTION

Recently, various types of 3D NAND with a poly-Si channel have been introduced for ultra-high-density data storage [1-3] (Fig. 1). These structures mainly utilize a junction-free virtual S/D structure (without heavily doped S/D junctions) because conventional junction implantation is very difficult for a 3D stackable process. However, the loss of the read current due to high S/D resistance, which is induced by an insufficient fringing field and the nature of the poly-Si material, becomes problematic. This can also deteriorate due to the limit in scaling the equivalent oxide thickness (t_{EOT}). Additionally, 3D NAND structures with a floating body require careful consideration when designing S/D junctions for enhanced erase characteristics. To fix the floating body potential during erase operations effectively, a sufficient number of holes must be generated by band-to-band tunneling from the S/D junctions. Therefore, the S/D junctions need to be heavily doped, abrupt, and uniform. Unless 3D NAND structures satisfy the aforementioned demands, uniform and efficient erase characteristics cannot be ensured in conventional diffused S/D and junction-free virtual S/D structures. (Fig. 2).

For the first time, this work demonstrates a novel 'junctionless' all-around-gate (AAG) SONOS device with homogeneously n^+-doped quantum-scale single-crystal silicon nanowire (SiNW) for 3D NAND Flash. Nominal dimensions are a diameter (d_{NW}) of 4 nm and a gate length (L_G) of 20 nm. It should be noted that program inhibition can be easily attained by the direct raising of the unselected bit-line potential because the homogeneously n^+-doped SiNW (> 10^{19} cm^{-3}) string can serve as a buried bit-line; hence, self-boosting [4] is unnecessary. Additionally, the junctionless AAG devices provide the extra benefits of an improved read current, a uniform erase V_T distribution, and improved endurance behaviors.

DEVICE FABRICATION

A schematic and the nominal device parameters are shown in Fig. 4. The SiNWs are fabricated by a one-route deep RIE process (Bosch process [5]). The process flow and TEM photographs are displayed in Figs. 5 and 6, respectively. For n^+-doped SiNW channels, high dose implantation is applied before the Bosch process. Note that there are no additional complex S/D implantation and gate spacer processes. The TEM images confirm a 4 nm d_{NW}, a 20 nm L_G, and thicknesses of the O/N/O layers of 2.8/6.2/7 nm. Conventional inversion-mode devices with diffused S/D junctions were also fabricated here as a control group for a fair comparison.

RESULTS AND DISCUSSIONS

The transfer and V_T roll-off characteristics of the fabricated junctionless AAG SONOS devices are shown in Figs. 7 and 8 for different L_G values. A high I_{ON} (~10 μA) with a t_{EOT} value of 14 nm was achieved. In the junction-free virtual S/D structure, a large pass gate voltage is necessary for a higher I_{ON}, resulting in severe pass disturbance. In the junctionless device, however, it should be noted that the I_{ON} current is mainly determined not by the gate capacitance but by the initial doping concentration of the SiNW channel. As a result, a high I_{ON} can be achieved naturally without pass disturbance arising. More to the point, a low negative V_T of junctionless devices can favorably increase the disturbance margin.

Fig. 9 shows P/E transient characteristics of junctionless AAG SONOS devices with a 20nm L_G and a 4 nm d_{NW} for various P/E conditions. A large P/E window (ΔV_T) up to 6.5 V was attained with the aid of a GAA structure despite the highly scaled device size, demonstrating the cell suitability for MLC operations. No erase saturation phenomenon was observed, even at -15V despite the n^+ poly-Si gate. This indicates that there is no need to use a metal-gate or high-k blocking oxide. Moreover, in Fig. 10, program inhibition is achieved by the direct raising of the unselected bit-line potential. It is implicit that there is no need to introduce a complex self-boosting method. A high incremental step pulse program (ISPP) slope (0.7) is also attained, even with a L_G value of 20 nm. Fig. 11 shows the typical read disturbance under stresses. All disturbed cells can be readily controlled within V_T < 0V due to the low initial V_T.

Fig. 12 compares the distribution of the erased V_T for the junctionless and inversion-mode AAG SONOS devices. As mentioned earlier, the erase characteristics of the floating body cell are strongly determined by the profiles of the S/D junctions. Contrary to inversion-mode devices, the S/D of junctionless devices is precisely controlled by the gate electric field. As a result, a uniformly distributed erased V_T is successfully obtained without any V_T correction methods.

Because the conduction of a junctionless device initially occurs in the center of an n^+-doped SiNW channel, it can be less sensitive to the interface trap generated from P/E cycles compared to a conventional inversion-mode device, as shown in Fig. 13. In a TCAD simulation, we confirmed that the acceptor-type interface trap does not significantly affect the V_T shift in a junctionless device. Note that the higher the doping concentration of a SiNW channel is, the stronger the P/E endurance becomes. Reasonable post-cyclic data retention characteristics were achieved, as also shown in Fig. 13.

The proposed deep RIE process was applied to implement vertically integrated 9-layer single-crystal SiNWs on a bulk-Si wafer. This was enabled by iterative plasma etching processes to separate each of the 9 SiNWs. Their SEM and TEM images are shown in Fig. 14. Projecting from these results, promoting high throughput and a lower cost per bit is feasible for high-performance memory characteristics.

CONCLUSIONS

A novel junctionless AAG SONOS device with quantum-scale (4 nm d_{NW} and 20 nm L_G) was demonstrated in this work. A high I_{ON} value, good DC characteristics, a large ΔV_T, a narrow distribution of the erased V_T, and strong P/E endurance were achieved. Moreover, the fabrication of vertically integrated 9-layer single-crystal SiNWs was successfully demonstrated by the deep RIE processes. The results reveal that the structure of a junctionless device with a multi-layered SiNW is highly promising for future high-density 3D NAND.

REFERENCES

[1] R. Katsumata et al., *VLSI Tech. Dig.,* p.136, 2009. [2] J. Jang et al., *VLSI Tech. Dig.*, p.192, 2009. [3] W. Kim et al., *VLSI Tech. Dig.,* p.188, 2009. [4] K. D. Suh et al., *IEEE Journal of Solid-State Circuits*, p.1149, 1995. [5] F. Laermer et al., US-Patent No. 5501893.

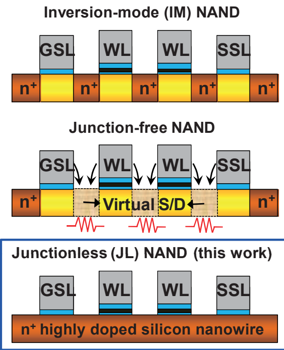


Fig. 1. Previously reported 3D NAND structures (conventional diffused S/D and junction-free virtual S/D) and the proposed 3D NAND structure (junctionless with a highly n^+-doped SiNW channel)

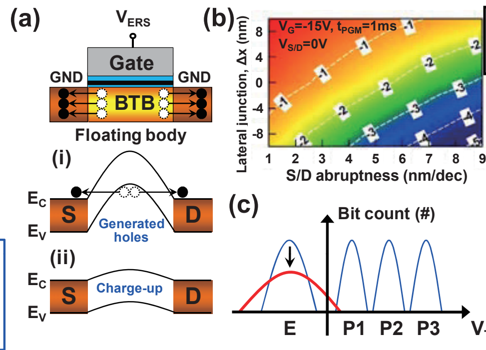


Fig. 2. (a) Erase operations for the 3D NAND structure with a floating body: (i) First, the floating body potential follows the gate potential (V_{ERS}). As a result, holes are generated from band-to-band tunneling. (ii) Second, the generated holes can pin the floating body potential. (b) TCAD simulation of the floating body potential during an erase operation. (c) Non-uniform S/D junctions can result in a broadened distribution of the erased V_T values.

ACKNOWLEDGEMENT This work was supported by the IT R&D program of MKE/KEIT [10035320, Development of novel 3D stacked devices and core materials for the next generation flash memory].

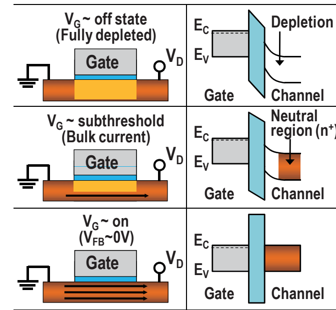
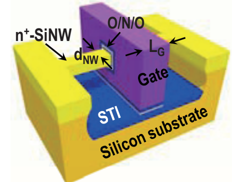


Fig. 3. Operational principle of the junctionless device. Because the junctionless device with a highly n^+-doped SiNW is normally in the on-state, the SiNW channel itself can serve as a buried bit-line.



L_G (nm)	20 ~ 50
d_{NW} (nm)	4
O/N/O (nm)	2.8 /6.2/ 7
N_{si} (/cm³)	5×10^{18} ~ 1×10^{19}
Gate	n^+ poly

Fig. 4. Schematic and nominal parameters of the proposed junctionless AAG SONOS device.

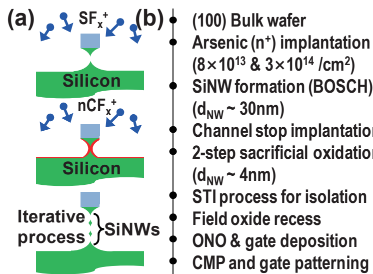


Fig. 5. (a) The method used to form a SiNW by the deep RIE process. (b) Process flow of the junctionless AAG SONOS device.

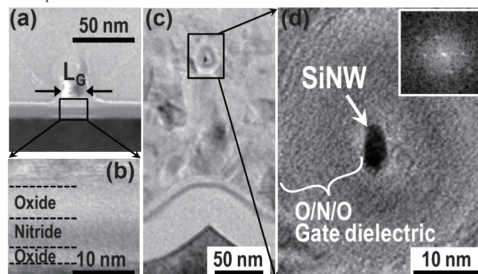


Fig. 6. (a) A TEM image of the fabricated device along the gate length direction. (b) A magnified TEM image of the O/N/O layers. (c) A TEM image perpendicular to the gate length direction. (d) A magnified TEM image of Fig. 6(c).

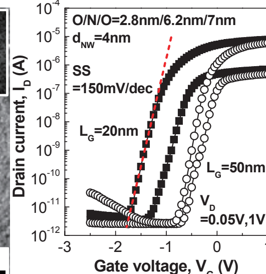


Fig. 7. Transfer characteristics of the junctionless AAG SONOS device with a 4 nm d_{NW} and a 20 nm L_G.

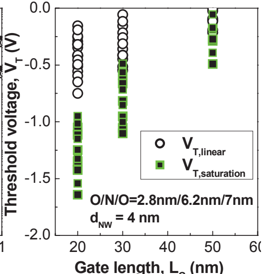


Fig. 8. V_T versus various gate lengths as a parameter of the drain voltage (0.05V and 1V)

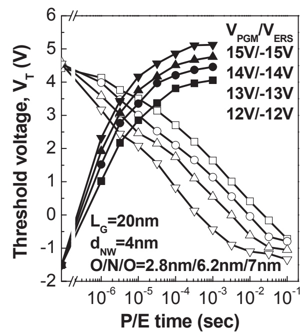


Fig. 9. Program and erase transient characteristics of the junctionless AAG SONOS device.

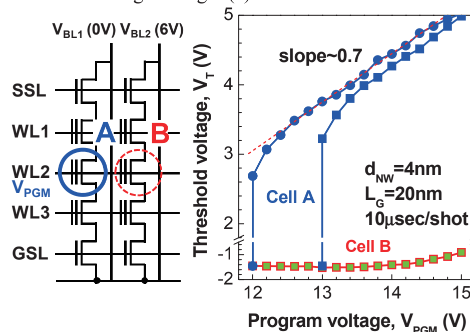


Fig. 10. ISPP programming and related inhibit method. Program inhibition is achieved by directly raising the unselected bit-line potential. For a programmed cell, a higher incremental step pulse program (ISPP) slope is also attained, even at 20 nm L_G.

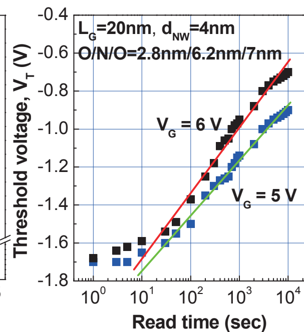


Fig. 11. Read disturbance evaluation of the junctionless AAG SONOS device.

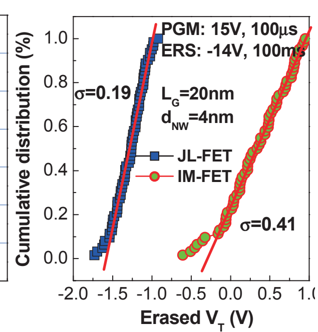


Fig. 12. Distribution of erased V_T values for junctionless and inversion-mode AAG SONOS devices.

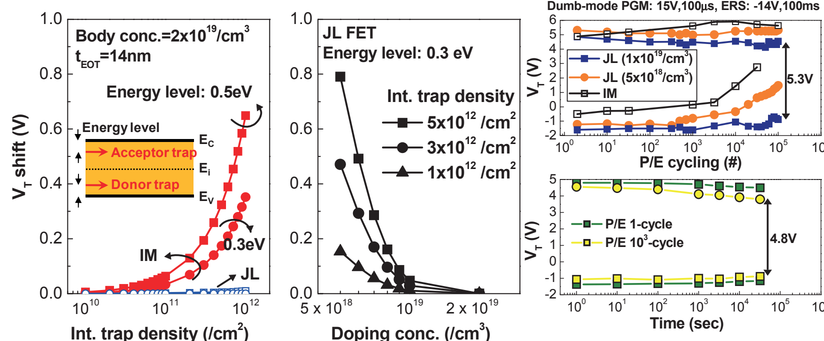


Fig. 13. (a) Simulated V_T shift versus interface trap density (N_{it}) as a parameter of the energy level of both acceptor- and donor-type traps. (b) Simulated V_T shift versus doping concentration of the SiNW channel in the junctionless device. The SiNW channel with higher n-type doping concentration shows a smaller V_T shift. (c) Dumb-mode P/E cycling (without any P/E verify) endurance test. (d) Post-cycling retention characteristics of the junctionless device.

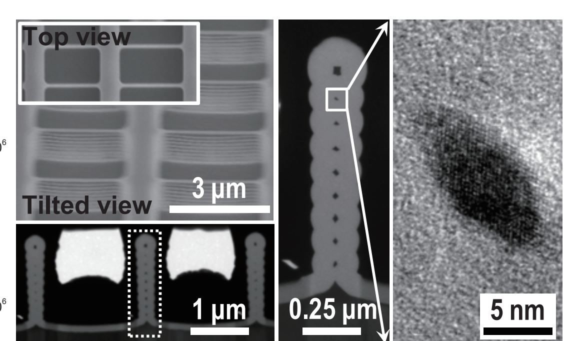


Fig. 14. SEM/TEM images of the fabricated 9-layer single-crystal SiNWs. The iterative deep RIE processes enable the formation and separation of each SiNW. The magnified TEM image confirms that the fabricated SiNW is not degraded by the etching steps.