Metal source/drain technology for nanoscale MOSFET & high speed flash applications

Moongyu Jang[1], Myungsim Jun[1], Yangkyu Choi[2] and Seongjin Choi[1, 2]
[1] Electronics & Telecommunications Research Institute (ETRI), Daejeon, Korea
[2] Korean Advanced Institute of Science & Technology (KAIST), Daejeon, Korea
jangmg@etri.re.kr

Abstract

Metallic source/drain technology is widely investigated including MOSFETs, single electron transistors, flash memories and thin film transistors. Due to the existence of Schottky barrier between metallic silicide and silicon, the subthreshold swing characteristic is enhanced and the source/drain parasitic resistance is reduced giving the improvement of device characteristics. Also, due to the tunneling process through the Schottky barrier, the flash memory characteristic is dramatically enhanced.

Introduction

As the feature sizes of the conventional field-effect-transistors (FETs) continue to shrink into the nanometer regime, physical and technological problems such as short-channel effects and dopant fluctuation issues are significant emerging problems. Tunnel transistors with metallic source and drain structures have attracted attentions because the aforementioned problems could be overcome. For example, in nanotube/nanowire devices, such CNT FETs, silicon and ZnO nanowire FETs, etc, metallic electrodes (Au, Ti, TiN, etc.) are widely being used as the source and drain materials. In metallic source & drain devices, the main charge transport mechanism is tunneling through the Schottky barrier existing between the metal and semiconductor interfaces.

In this paper, various sizes of Schottky barrier MOSFETs (SB-MOSFETs) are manufactured down to 7nm using erbium-silicide and platinum silicide for n-/p-type transistors. Also, the short channel characteristics of SB-MOSFETs are analyzed using SS characteristics to check the scalability. Moreover, the low temperature (7K) behavior is also investigated to check the possibility as single electron transitor.

Here, also, we demonstrate a new type of Flash memory cell based on the structure of dopant-segregated Schottky-barrier (DSSB) MOSFET. The hot carriers intrinsically generated from the shallow DSSB source/drain junctions can be utilized for the advancement of both the NAND and the NOR type Flash memory cell. With the aid of these hot carriers that possess improved probability to be trapped into a charge storage node such as polysilicon layer in the floating gate memory device or the nitride layer in the SONOS memory device, the DSSB MOSFET shows very fast programming time at low programming voltage, compared to conventional MOSFET based on p-n S/D junctions. Besides, the superior scalability resulting from the abrupt and shallow junctions are also achieved without the constraint of the parasitic resistance due to metallic silicided material. Furthermore, the DSSB thin film transistor based on polycrystalline silicon for the application of 3-D stackable memory will be reported.

Results and Discussions

Erbium and platinum are chosen as source/drain metal of n/p-type SB-MOSFETs, because of its low Schottky barrier height for electrons and holes, respectively. Devices are fabricated with the procedures as following. After gate etching, 15nm thin spacer is made using 900℃ thermal oxidation method. Erbium-silicide and platinum-silicide are formed on low doped ($N_{SUB}=10^{15}cm^{-3}$) SOI layer by annealing at 500℃ for 10min using rapid thermal annealing method. The remained erbium and platinum are removed using sulfuric Peroxide mixture (SPM) and aqua regia for 10min, respectively. Fig. 1 shows the diode characteristics of $ErSi_{1.7}$ on p-sub and PtSi on n-sub, respectively. The extracted Schottky barrier height of $ErSi_{1.7}$ for hole is 0.77eV and PtSi for electron is 0.87eV which corresponds to 0.36eV for electron and 0.25eV for hole, respectively.

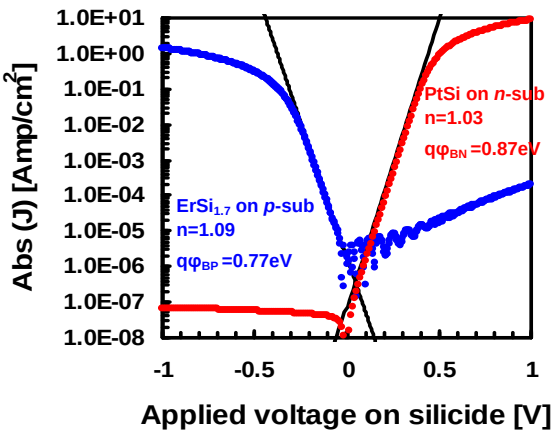

Fig. 1. Schottky diode I-V characteristics

Fig. 2 shows I_{DS}-V_{GS} and I_{DS}-V_{DS} characteristics of the 20 ㎛ long channel n/p-type SB-MOSFETs. The gate oxide and spacer thickness is 5nm and 15nm, respectively. Both the n/p-type SB-MOSFETs show high on/off current ratio, larger than $I_{on}/I_{off}>10^5$ with low leakage current (I_{LKG}<100 pA/㎛). The on/off ratio and the leakage current level is the highest and lowest values compared with previously published data in SB-MOSFETs. Also, DIBL is almost suppressed in both n/p-type SB-MOSFETs and the SS value is 60mV/decade both in n-type & p-type SB-MOSFETs, reaching the theoretical limit value in MOSFETs .

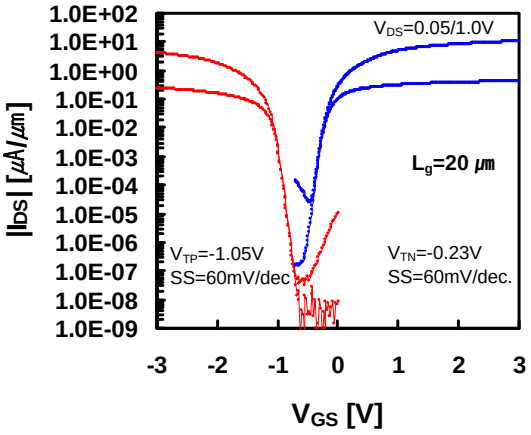

Fig. 2. I_{DS}-V_{GS} characteristics of 20μm *n/p*-type SB-MOSFET.

Fig. 3 shows the IDS-VGS characteristics of 7nm gate length n-type SB-MOSFETs manufactured on n-type substrate. Still the off-state leakage current is less than 0.1uA/um due to the existence of Schottky barrier between source and silicon. The degradation of characteristic is mainly due to the increased gate oxide thickness caused during sidewall oxidation process.

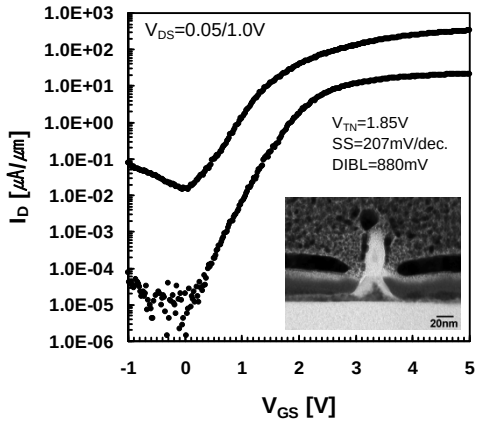

Fig. 3. I_{DS}-V_{GS} characteristics of 7 nm n-type SB-MOSFET.

Fig. 4 shows the cross-sectional view of manufactured DSSB MOSFET. TEM image across a-a' and b-b' direction correspond to the left and right figure, respectively. The sidewall spacer is observed as shown in left figure. Fabricated fin widths are from 30nm to 100nm, and the height of fin is 75nm. The recessed source and drain structure is formed by etch-back process.

Fig. 5 shows the programming characteristics between conventional and DSSB FinFET SONOS memory. DSSB device shows dramatically improved programming characteristics. If we set the targeting threshold voltage as 4 V, the programming time is faster than 1,000 times compared with conventional device. This enhanced programming characteristic of DSSB device is mainly due to the existence of Schottky barrier which causes the injection of more energetic carrier at the edge of source region due to the tunneling process through the Schottky barrier.

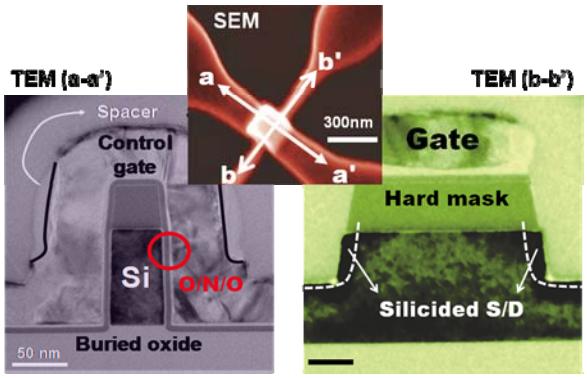

Fig. 4. Fabricated DSSB FinFET SONOS

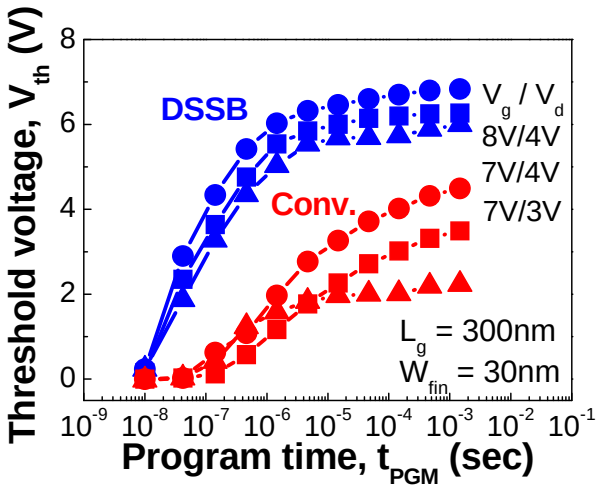

Fig. 5. Comparison of programming characteristics between conventional and DSSB FinFET SONOS.

Conclusions

In summary, metallic source/drain technology is widely investigated including MOSFETs, single electron transistors, flash memories and thin film transistors. The metallic source/drain structured devices are a very promising candidate for future nano-electronics applications of the logic and Flash memory device since they enable the continuation of device scaling.

References

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