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Current Flow Mechanism in Schottky-Barrier MOSFETs and Application to the 1T-DRAM

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ABSTRACT

The current flow mechanism in Schottky-Barrier MOSFETs (SB-MOSFETs) is investigated. A method to examine the current flow mechanism is developed and verified through comparison of measurement results with simulation data. Using the developed method, it was found that the off-state current flow mechanism is changed from tunneling (TU) to thermionic emission (TE) as the back bias (V_{bs}) increases due to lowered Schottky barrier height. Finally, by using this mechanism, a novel operation scheme for the 1T-DRAM is provided.

INTRODUCTION

SB-MOSFETs have been considered as an alternative to conventional MOSFETs due to their excellent short-channel effect immunity and low parasitic components **[1]**. The on-state transport mechanism has also been widely researched, whereas the off-state transport has seen relatively less studied. Since the mechanism for the off-state current in SB-MOSFETs is physically different from that in conventional MOSFETs, it is timely to study the current flow mechanism of the off-state. In this study, PMOS and NMOS by using PtSi and ErSi were fabricated. A refined effective extraction method of Schottky-Barrier-Height (SBH) is developed and then verified through comparison with numerical simulation data. The dominant transport in the off-state associated with the V_{bs} is investigated. Finally, the fabricated SB-MOSFETs are applied to the 1T-DRAM by using this mechanism.

EXPERIMENTS

A schematic of the device and process flow are shown in **Fig. 1** and **Fig. 2**, respectively. **Fig. 3** also shows a STEM image of SB-MOSFETs. The measured sheet resistance for PtSi and ErSi is 15 ohm/square, although the line width is narrower than 120nm. A numerical simulation is carried out with consideration of TU and TE transport models for analysis. Temperature characteristics were measured with a hot-chuck system from 300K to 450K.

RESULTS AND DISCUSSIONS

Fig. 4 and **Fig. 5** show the transfer and output characteristics for the fabricated PtSi p-type SB-MOSFETs, respectively.

Extraction method of effective Schottky barrier height – The effective SBH is extracted by varying the substrate temperature as shown **Fig. 6**. The effective SBH by considering TE is given by the slope of an Arrhenius plot ($\ln(I_{ds})$ vs. 1000/T for given V_{gs}). Unlike conventional MOSFET where the subthreshold current is dominated by diffusion, in SB-MOSFETs, it is dominated by TE. In subthreshold region, high barrier height blocks the injection of carriers into the channel. As V_{gs} increases negatively in the PMOS, the barrier reduces, and carriers have sufficient thermal energy to surmount the barrier. Subsequent increased current with V_{gs} is due to tunneling through the barrier **[2]**. On the other hand, back-tunneled electrons in PMOS are the dominant factor of leakage current, because electrons in the drain side can tunnel through the barrier. The extracted SBH clearly shows these phenomena. In **Fig. 6**, the subthreshold region shows a linear slope until Φ_{Bp} of PtSi=0.25eV. Then it is changed beyond $|V_{gs}|>-1V$. It can thus be deduced that the dominant mechanism changes from TE to TU as V_{gs} negatively increases over the V_{th}. This was also suggested from a comparison of the inversion charge density and thermal energy **[3]**. Furthermore, effective SBH becomes lower as $|V_{gs}|$ increases in the off-state, which arises from electron back-tunneling in drain side. This shows that the dominant factor of the leakage is not TE but TU. Additionally the absolute slope increases and the peak barrier height for holes lowers as $|V_{ds}|$ increases. This is because a large $|V_{ds}|$ can induce high tunneling probability due to narrower tunneling width in the drain and lowers the peak barrier, which is consistent with increased leakage. In the case of thick spacer thickness, however, the on-state TU was not observed due to poor gate controllability at the underlap region between source and channel. The thicker spacer shows lowered tunneling, as shown in **Fig. 7**. As a result, the effective SBH stays constant near 0.25eV (Φ_{Bp} of PtSi) at V_{gs}<-1V (i.e. on-state). It is deduced that TU is not the dominant transport mechanism in the case of a thick spacer at the on-state. In addition, leakage does not depend on V_{gs} due to the thick spacer (i.e. almost constant effective SBH in the off-state).

Back bias effect on SB-MOSFET – The spacer thickness is a crucial parameter for a high current drivability. This is illustrated in the inset of **Fig. 7**. In the channel below the spacer, the hole (PMOS) cannot be sufficiently inverted, thus leading to large series resistance. **Fig. 8** exhibits that $|I_{ds}|$ increases as the V_{bs} increases negatively. The channel at the underlap can be inverted as V_{bs} induces negatively. Therefore, the lowered drive current due to the thick spacer thickness can be solved by applying proper V_{bs}. In the case of a thin spacer thickness, however, $|I_{ds}|$ no longer increases, as shown in **Fig. 8**. Furthermore V_{bs} affects the leakage mechanism as well. In general, the origin of leakage is the back tunneling from the drain side **[4]**. As V_{bs} negatively increases in the PMOS, the mechanism governing the off-state is changed from TU to TE, as shown in **Fig. 9.** At large negative V_{bs}, the off-state current suddenly increases due to the lowered hole barrier, as shown in **Fig. 10**. As low V_{bs} is negatively induced in the PMOS, the leakage current due to TU from the drain side is generally reduced, because the tunneling width is increased near the t_{ox}/channel interface, even though it depends on the buried oxide thickness and body thickness. As high V_{bs} is negatively induced, however, the leakage current by TE is increased by the lowered hole barrier for the PMOS. In this case, the leakage current path changes from the channel interface to the BOX interface due to the lowered hole barrier. This means that the leakage current mechanism is changed from TU of electrons to TE of holes. This phenomenon is verified via a numerical simulation. As shown in **Fig. 11,** good agreement is attained between the measured data and simulation data. **Fig. 12** also shows that peak barrier height is lowered due to V_{bs}, which results in increment of the leakage current by TE.

Possibility on 1T DRAM – As noted above, the off-state current is increased due to TE upon applying large V_{bs}, and this scheme can be applied to 1T DRAM. This concept is verified by using a NMOS (i.e. ErSi S/D). In the off-state, tunneled holes from the drain can be confined in the potential wall by using an appropriate negative V_{bs} as shown in **Fig. 13**. This results in an increase of the body potential, and subsequent increment of I_{ds} due to TE of electron (for NMOS) by lowered electron barrier (i.e. similar to hole barrier for PMOS). The I_{ds} difference can be sensed in the off-state at a low V_{gs} (i.e. by using ambipolar characteristics) so as not to change the sensing margin. In general, SB-MOSFETs have an ability to reduce impact ionization rates and floating body effects **[5]**. Therefore to operate 1T DRAM in a SB-MOSFET, the TU component of hole in off-state should be used to enhance the body potential. **Fig. 14** shows the measured value of source current. From a scalability point of view, SB-MOSFETs are expected to be good candidates for device and memory applications.

CONCLUSIONS

Schottky-Barrier MOSFETs are fabricated and the dependence of the back bias voltage on the current transport mechanism is analyzed. At the off-state, as the back bias increases, the current mechanism is changed by tunneling to thermionic emission mechanism. This thermionic current is used for an operation scheme of the 1T-DRAM.

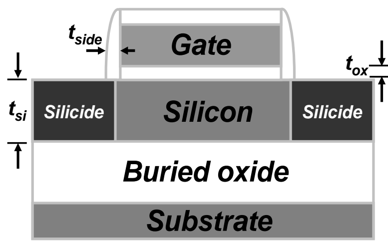

Fig 1. Device schematic of SB-MOSFET SOI device. The gate length (L_g) is 2.2μm and the gate oxide thickness (t_{ox}) is 10nm. The body thickness is 50nm.

- Body thinning (t_{si}=50nm)
- Active region patterning
- Gate oxidation (t_{ox}=10nm)
- N+ poly silicon deposition (250nm)
- LP TEOS deposition (150nm)
- Gate patterning
- Spacer formation (30nm)
- Pt, Er sputtering (50nm)
- Thermal process (silicidation)
- Unreacted metal removal

Fig 2. Process flow of SB-MOSFET. Silicidation process is accomplished by rapid thermal process. Unreacted metal is removed by using aqua regia for Pt, and SPM for Er

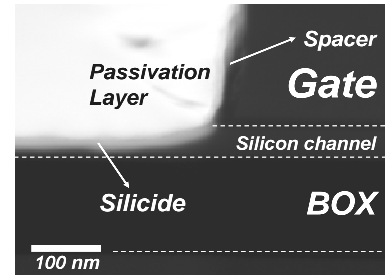

Fig 3. Scanning Transmission Electron microscope (STEM) image of PtSi SB-MOSFETs

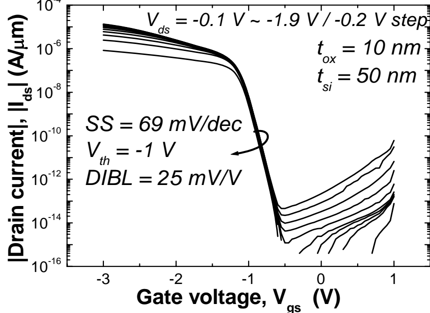

Fig 4. Transfer characteristics of SB-MOSFET. Threshold voltage is -1V (constant method), and SS and DIBL are 69mV/dec and 25mV/V, respectively

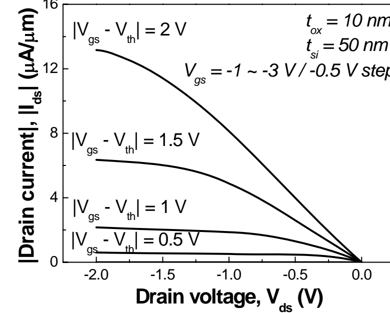

Fig 5. Output characteristics of SB-MOSFET. The current is normalized by the channel width.

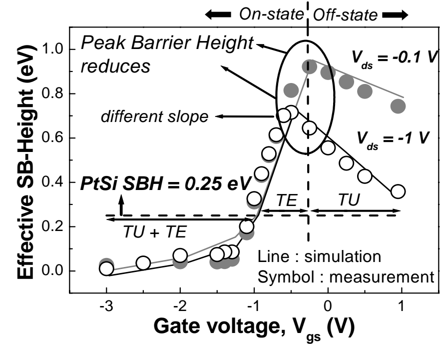

Fig 6. Extraction of effective SB-height. The slope in the off-state represents the tunneling probability. As $|V_{ds}|$ increases, the slope increases.

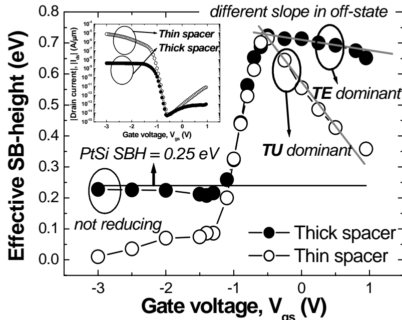

Fig 7. Effective SBH comparison. Thick spacer SB-MOSFETs have low hole tunneling probability in the on-state.

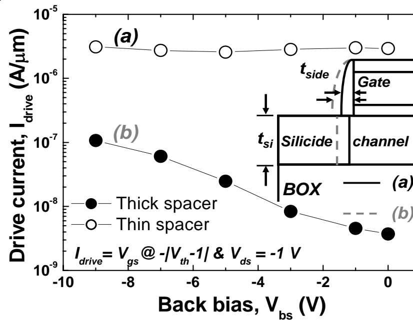

Fig 8. Comparison of I_{drive}. As V_{bs} increases, the underlap between the source and the channel is inverted. Therefore, I_{drive} increases in thick spacer.

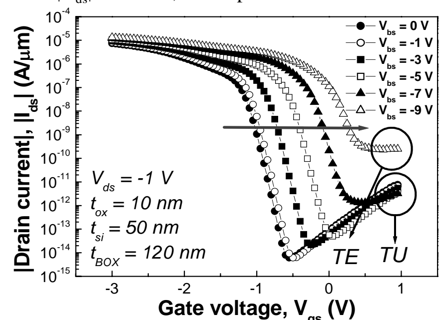

Fig 9. Measured characteristics corresponding to different V_{bs}. If V_{bs} is induced positively, the hole TE current increases due to the lowered barrier.

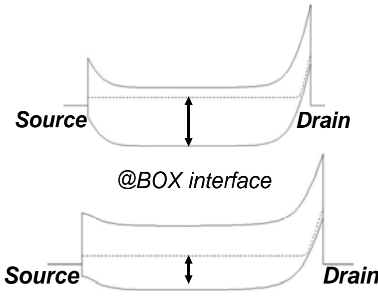

Fig 10. Explanation of simulated band-diagram. At the BOX interface, the hole barrier is lowered as V_{bs} is applied negatively.

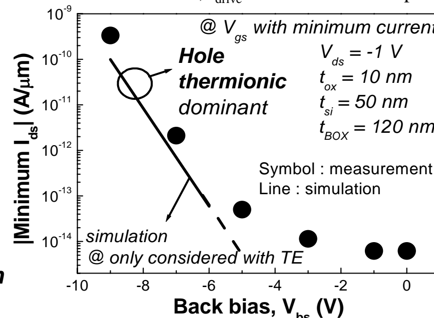

Fig 11. Minimum current comparison between measured and simulated data. Measured data show the good agreement with simulation results, where only the thermionic model is consiered.

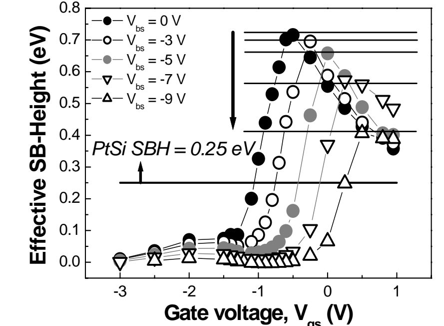

Fig 12. Extraction of SBH. As back bias is applied, the peak barrier is lowered, and the slope in the off-state is decreased.

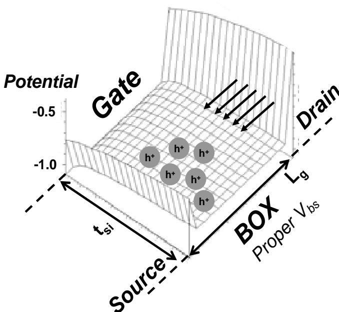

Fig 13. Simulated potential wall. Holes from the drain side can be tunneled and are confined at the body. This causes increment of the body potential, and the increment of subsequent I_{ds}.

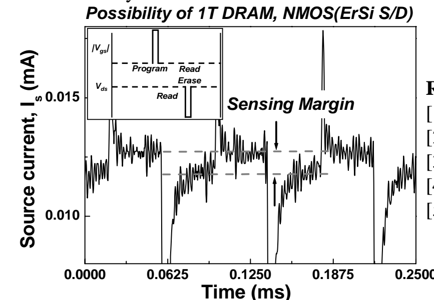

Fig 14. Possibility of capacitorless DRAM. Using the increment of the body potential due to the tunneled hole, 1T DRAM can feasibly operate with a non-destructive read condition.

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