Band Offset FinFET-Based URAM (Unified-RAM) Built on SiC for Multi-Functioning NVM and Capacitorless 1T-DRAM

Jin-Woo Han[1], Seong-Wan Ryu[1], Sungho Kim[1], Chung-Jin Kim[1], Jae-Hyuk Ahn[1], Sung-Jin Choi[1], Kyu Jin Choi[2], Byung Jin Cho[1]
Jin Soo Kim[3], Kwang Hee Kim[3], Gi Sung Lee[3], Jae Sub Oh[3], Myong Ho Song[3], Yun Chang Park[3], Jeoung Woo Kim[3], and Yang-Kyu Choi[1]
[1]EECS, KAIST, Daejeon, Korea, [2]Jusung Engineering, Gwangju, Korea, [3]National Nanofab Center, Daejeon, Korea
E-mail: ykchoi@ee.kaist.ac.kr, Phone: +82-42-869-3477, Fax: +82-42-869-8565

Abstract

A FinFET-based unified-RAM (URAM) using the band offset of Si/SiC is demonstrated for the fusion of a non-volatile memory (NVM) and capacitorless 1T-DRAM operation. An oxide/nitride/oxide (O/N/O) gate dielectric and a floating body caused by the band offset are combined in a bulk FinFET to allow two memory operations in a single transistor. The device is fabricated on an epitaxially grown Si/SiC substrate and its process is fully compatible with a conventional bulk FinFET SONOS. Highly reliable NVM and high speed 1T-DRAM operation are confirmed in a single URAM cell.

Introduction

In the digital convergence era, the development of multi-functional or fusion memory holds particular attraction [1-3]. An example of fusion memory, NVM and 1T-DRAM can be operated in a single memory cell, and these operations are identified by the bias conditions of V_g and V_d as shown in **Fig. 1**. We recently proposed a FinFET SONOS URAM fabricated on a SOI substrate [3]. However, the SOI substrate is prone to heat dissipation, which degrades the sensing window for 1T-DRAM [4]. In the present work, we propose a band offset URAM architecture built on Si/SiC for effective management of heat and reduced fabrication cost.

A buried n-well layer that serves as a barrier to hold holes has been employed in a bulk substrate for 1T-DRAM whereas a buried oxide has been used in SOI [5-6]. However, with the deep implantation process for the buried n-well, it is difficult to accurately define the abrupt doping profile. Thus, epitaxially grown Si/SiC to hold holes by the band offset is proposed. A FinFET-based URAM is also fabricated on a buried n-well as a control group.

Device Fabrication

The process sequence is summarized in **Fig. 2**. First, a $Si/Si_{0.99}C_{0.01}$ layer is epitaxially grown for the band offset, and buried n-implantation is carried out in the case of the control group. The subsequent steps correspond with those of the bulk FinFET SONOS process flow [7]. The fabricated device dimensions and parameters are summarized in **Table 1**. SEM/TEM images are shown in **Fig. 3**. Si/SiC lattices are perfectly matched as shown in the fast Fourier transformed images. The SIMS profile for the buried n-well device is shown in **Fig. 4**.

Results and Discussion

NVM characteristics - **Fig. 5** shows the speed response of P/E carried out by a FN-tunneling mechanism. Both devices show similar threshold voltage (V_T) shift. **Fig. 6** shows the reliability characteristics. 10 year retention behaviors are observed along with a more than 3V V_T window; however, the Si/SiC device shows better data retention time. In addition, excellent endurances of more than 10^7 P/E cycles are observed without V_T window degradation for both devices.

1T-DRAM characteristics – A floating body effect in bulk devices is originated from the buried n-well or the valence band offset of Si/SiC. **Fig. 7** shows the 1T-DRAM operation mechanism. For programming, the holes generated by impact ionization are stored in the Si body on band offset. For erasing, accumulated holes are eliminated by the forward biased drain. As evidence of holes accumulation, a kink appears in the I_D-V_D curves, as shown in **Fig. 8**. A simulated contour of the hole concentration in **Fig. 9** clearly shows that both the buried n-well and the band offset of Si/SiC can store holes. **Fig. 10** shows the P/E characteristics for the 1T-DRAM operation.

Fig. 11 shows the P/E speed response. The Si/SiC device exhibits a wider sensing window than the buried n-well device. At $\tau_{PGM}=\tau_{ERS}=20$nsec, the sensing window in Si/SiC ($\Delta I_S=10\mu A$) allows a retention time of 50msec whereas the buried n-well ($\Delta I_S=6\mu A$) retains data during 10msec. If the retention time is increased, faster operation can be possible because of the saved refresh time. One important advantage in bulk devices is a tunable substrate voltage. By modulation of the substrate voltage, the barrier height to hold holes can be adjusted. As shown in **Fig. 12**, positive V_{SUB} ($0.1V<V_{SUB}<0.3V$) raises the barrier height resulting in increment of the retention time. In contrast, $V_{SUB}>0.4V$ reduces the retention time due to a forwardly biased substrate-drain junction. Although doubled retention time was observed in the buried n-well device by optimal V_{SUB}, Si/SiC still shows superior performance to the buried n-well device. Furthermore, these characteristics the Si/SiC device can be improved by increment of the content of C in SiC, as this will provide an enlarged valence band offset [8]. Impact ionization for 1T-DRAM programming can adversely stimulate charges to be trapped in the O/N/O layer, and consequently an undesired soft program can be possible in NVM. In order to examine interference between these two operations, I_D-V_G characteristics are compared before/after 1T-DRAM operation. As shown in **Fig. 13**, interference by the impact ionization is found to be negligible.

Conclusions

A band offset FinFET-based unified-RAM (URAM) on Si/SiC substrate is demonstrated. URAM performs NVM and 1T-DRAM functions in a single transistor with benefits of low cost and high heat dissipation. NVM uses an O/N/O layer for charge trapping, and 1T-DRAM utilizes a floating body effect for capacitorless DRAM operation in the bulk substrate.

References

[1] C. W. Oh *et al.*, *VLSI*, p.58, 2006. [2] C. W. Oh *et al.*, *VLSI*, p.168, 2007. [3] J.-W. Han *et al.*, *IEDM*, p.929, 2007. [4] P. C. Fazan, *et al.*, SPIE, p.489, 2002. [5] R. Ranica *et al.*, *VLSI*, p.38, 2005. [6] R. Ranica *et al.*, *VLSI*, p.128, 2004. [7] J. R. Hwang. *et al.*, IEDM, p.154, 2005. [8] H. J. Osten *et al.*, *JAP*, p. 2716, 1998.

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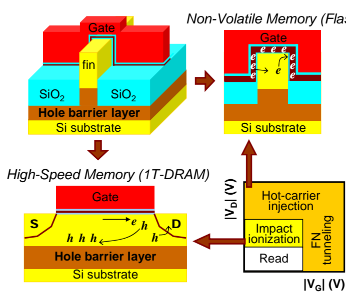
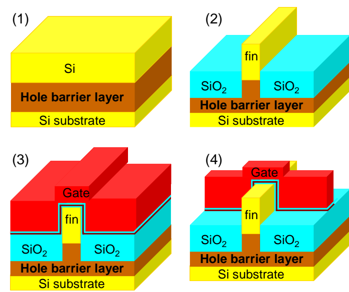


Fig. 1 : Schematics of URAM operation.



- (100) bulk wafer
- ***Si/SiC epitaxial growth***
  vs.
- ***buried n-well implantation***
- channel implantation
- fin patterning
- STI formation
- O/N/O and poly-Si formation
- gate patterning
- S/D formation

Fig. 2 : Process flow for bulk FinFET SONOS. An epitaxially grown Si/SiC layer or a buried n-well is used for the hole barrier.

Parameter	Si/SiC	Buried n-well
V_T (V)	0.11	0.18
DIBL (mV/V)	110	115
SS (mV/dec)	93	95
L_g (nm)	230	
W_{fin}(nm)	50	
H_{fin}(nm)	50	
$T_{O/N/O}$ (nm)	4/6/4	

Table 1 : Fabricated device dimensions and parameters of the measured device.

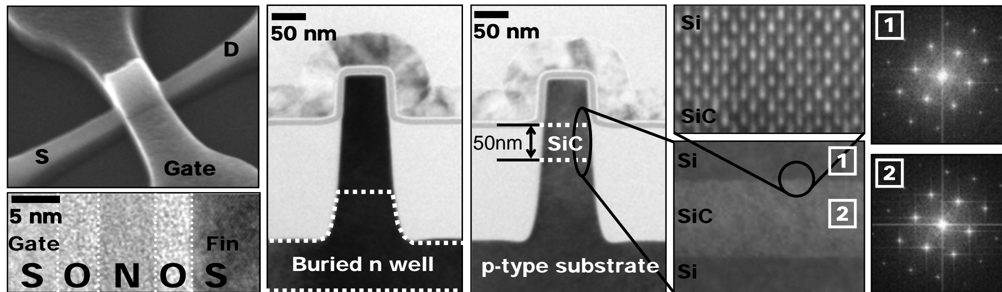


Fig. 3 : SEM/TEM images of the fabricated structure. Epitaxially grown $Si/Si_{0.99}C_{0.01}$ films show perfect crystallinity.

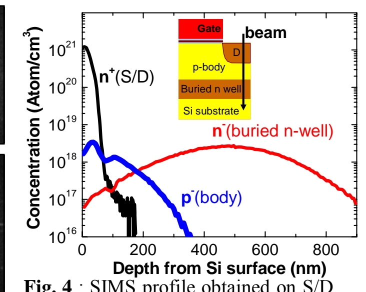


Fig. 4 : SIMS profile obtained on S/D to substrate region in buried n-well device.

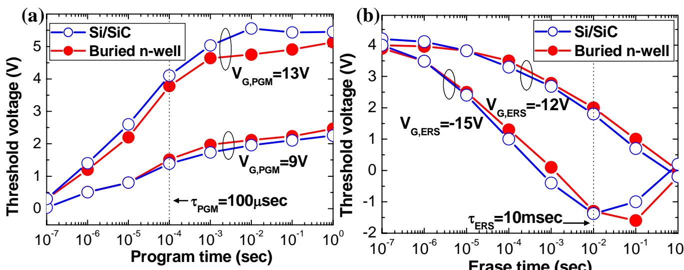


Fig. 5 : (a) Program and (b) erase speed characteristics for NVM operation. A FN tunneling mechanism is used for both program and erase.

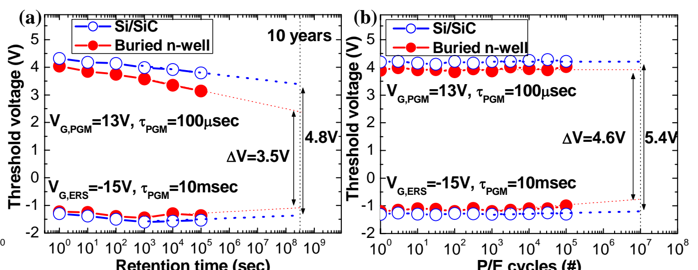


Fig. 6 : (a) Retention and (b) endurance characteristics for NVM operation. The Si/SiC device shows better retention characteristics. Both devices exhibit excellent endurance.

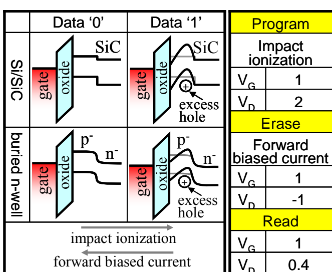


Fig. 7 : Schematic diagrams for P/E of 1T-DRAM and bias conditions used in this work.

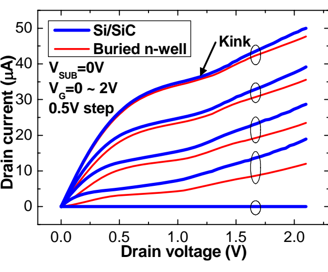


Fig. 8 : I_D-V_D characteristics. Kink ensures a floating body effect.

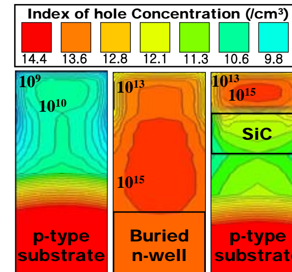


Fig. 9 : Hole concentration at impact ionization condition in Fig. 7.

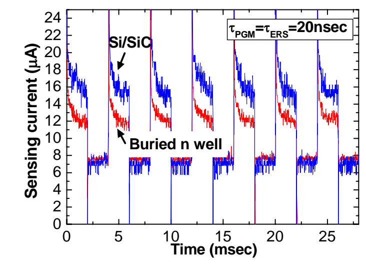


Fig. 10 : Program and erase characteristics for 1T-DRAM operation. Si/SiC shows a wider sensing window than buried n-well.

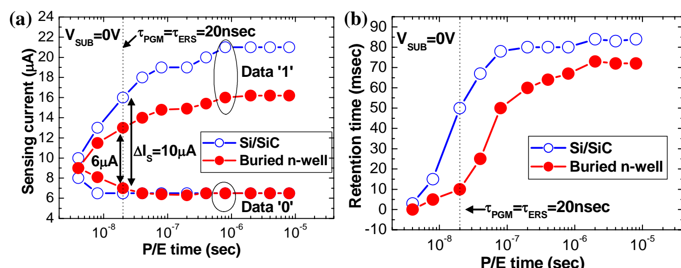


Fig. 11 : P/E speed for 1T-DRAM. (a) Data '1' state degradation is more severe than data '0' state. (b) Retention characteristics for 1T-DRAM. Si/SiC shows wider sensing window and longer data retention.

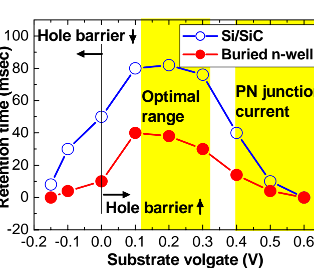


Fig. 12 : Retention time as a function of V_{SUB}. $0.1<V_{SUB}<0.3$ is optimal condition.

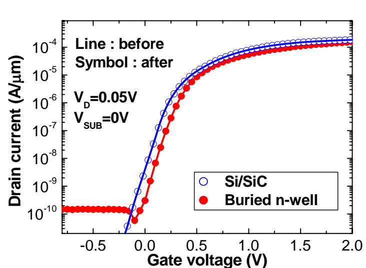


Fig. 13 : I_D-V_G curves before (lines) and after (symbols) 1T-DRAM programming.