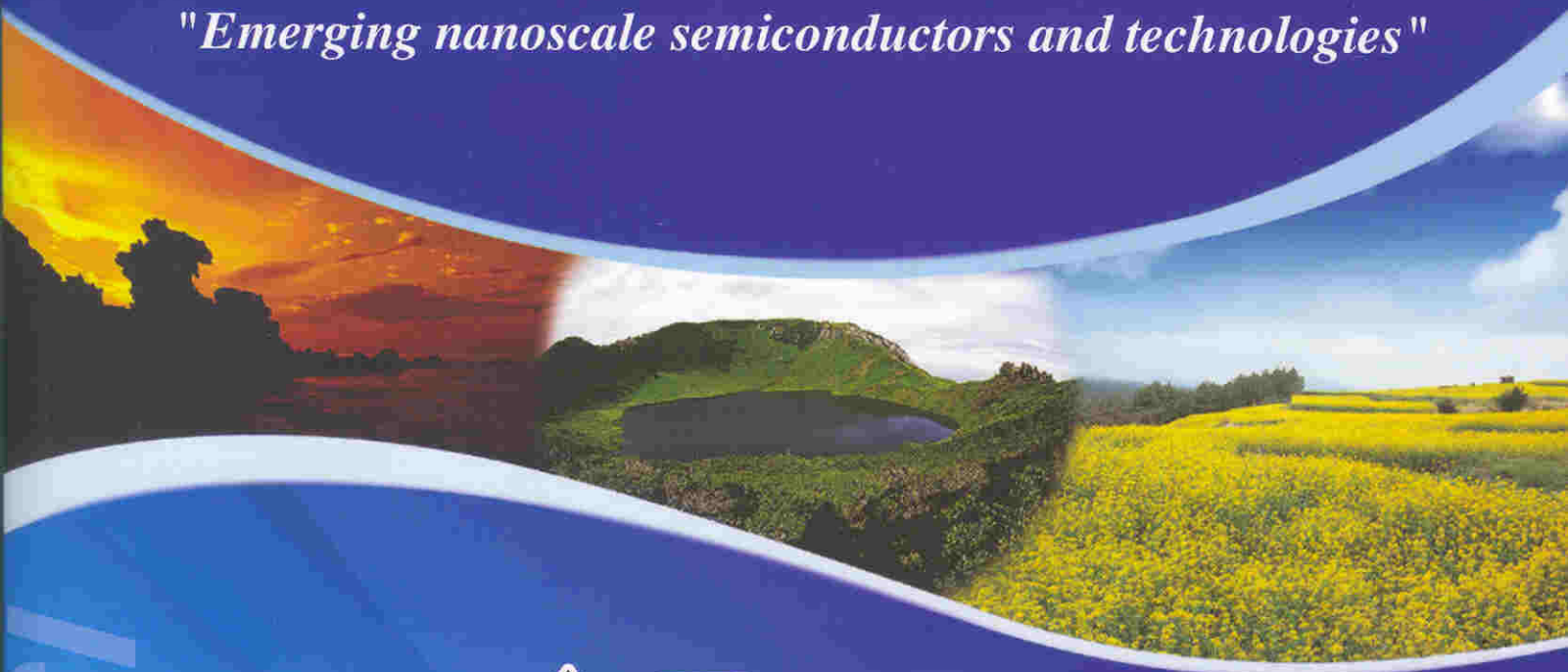
ABSTRACTS

The 14th International Symposium on the Physics of Semiconductors and Applications – 2008

"Emerging nanoscale semiconductors and technologies"



Yang-Kyu CHOI

August 26 – 29, 2008

Ramada Plaza Jeju Hotel, Jeju, Korea

http://ispsa2008.or.kr

Organized by

The Korean Physical Society (KPS)

KPS 한국물리학회 The Korean Physical Society

KOSEF LG-Inotech AIXTRON SAFC Hitech JEJU

ISPSA-2008

QMN-I-04

Evolutional Memory: Unified-Random Access Memory (URAM)

Yang-Kyu Choi* and Jin-Woo Han

School of EECS, Division of EE, Korea Advanced Institute of Science and Technology, Daejeon 305-701, Korea

For over last three decades, a semiconductor technology has been the basis of the Information Technology (IT) revolution. The silicon based memories such as DRAM, SRAM, and Flash have played a core role in an aspect of each domain: density, speed, and non-volatility for a semiconductor industry. The 'scaling' have been an important growth engine, which enables the exponential increase of density and the decrease of bit per cost. But the traditional scaling approach is now pushing these memories into a physical and a technological limit. For example, the state-of-the-art flash memory is being approached at the gate length down to 8nm, which was a fundamental limit of currently developed charge storage material [1]. This means that the revenue from the scaling is getting on the decrease by retard of the scaling.

In the future, a new paradigm will be required for creating the value and continuing the use of the infrastructure of the semiconductor industry. It is expected that a variety of functions as well as the device density will be a driving force to sustain the growth momentum in the silicon memory industry. For example, DRAM and flash memory functions can be operated in a single chip. Even though the concept of the fusion memory is already reported in the literature, this is a system level or package level fusion. Thus the difficulties in such fusion memory lie on the process and cost due to the dissimilar fabrication process of DRAM and non-volatile memory. In this paper, a new type of the fusion memory is presented. Unlike the traditional fusion memory, the DRAM and non-volatile memory function are integrated in a 'single memory transistor' [2]. This memory cell can operate as a DRAM mode for high speed operation and a flash mode for non-volatile application in the single memory transistor. By combining a floating body and oxide/nitride/oxide stacked gate dielectric, the high speed DRAM operation and the non-volatile memory operation is realized in the single transistor. Especially, the DRAM operation is feasible without a cell capacitor by using the floating body capacitor. According to an end-users' demand, one can allocate each operation to utilize each advantageous function. In summary, this paradigm shift from a multi-bit cell to the multi-function cell can make Moore's law be alive and continue an evolution of silicon technology.

[1] H. Lee et al., IEEE Symposium on VLSI Technology Digest of Technical Papers, pp. 114-115, 2007.

[2] J.-W. Han et al., IEEE International Electron Device Meeting, pp. 929-932, 2007.

*Yang-Kyu Choi , e-mail: ykchoi@ee.kaist.ac.kr, Tel: +82-42-869-3477, Fax: +82-42-869-8565