The Influence of Gate Poly-Silicon Oxidation on Negative Bias Temperature Instability in 3D FinFET

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Abstract

This paper presents the effects of gate poly-silicon oxidation (GPOX) on negative bias temperature instability (NBTI) in buried channel body-tied and SOI FinFETs for the first time using a measurement technique without a recovery during a NBT-stress test. Gate length dependency of the NBTI on FinFETs with GPOX is analyzed with various gate oxide thicknesses, stress biases, substrate biases, and device structures. In addition, the proposed revamped geometry-aware reaction-diffusion model explains the GPOX effects on 3D FinFET with gate length dependency.

Keywords: NBTI, On-the-fly, GPOX, FinFET, gate length dependency

Introduction

3-dimensional (3D) multi-gate FinFET structures are promising nano-scale devices with high robustness on short-channel effects and excellent scalability using conventional processes [1,2]. Additionally, a GPOX process is used to eliminate gate-induce drain leakage (GIDL) current by weakening the electric field in the drain-to-gate overlap region to reduce the off-state leakage current of a buried channel PMOS [3,4].

As the device is scaled down, the NBTI starts to limit the device performance and reliability more when compared to hot-carrier injection [5]. An NBTI measurement technique without recovery effects is important to understand the proper NBTI characteristics of 3D GPOX FinFETs [6-8].

Experiments

The schematics of a buried channel PMOS body-tied FinFET with GPOX is shown in Fig. 1. Detailed fabrication processes of body-tied FinFET and GPOX have been reported previously [2,9]. For NBT-stress measurement, a conventional stress-measurement-stress (SMS) method with device healing [7] and an on-the-fly (OTF) method with a gate/drain pulse to reduce recovery effects are used [8]. The gate oxide thicknesses (T_{ox}) of the body-tied FinFETs and the SOI FinFETs were 2.6nm and 5.8nm, respectively, when the GPOX thickness was 2.3nm at bulk silicon substrate.

Fig. 2 depicts the pulse-forms applied on the gate, drain, substrate, and source during a monitor- and stress-state. The gate and drain pulse were induced by a pulse generator (Agilent 81110A) and the linear region source current ($I_{SLin}=I_S$ @ $V_G=V_{TO}$-1V & V_D=-100mV) was monitored by a parameter analyzer (Agilent 4155B). Additionally, the source and substrate were grounded with a substrate temperature of 125°C. A V_{sub} of -0.2V was applied to the body-tied FinFET to ensure the virtual-floating body effects, which can mimic the SOI FinFET [10].

Results and Discussions

The linear source current (I_{SLin}) degradation of the buried channel body-tied FinFETs and SOI FinFETs with stress time is shown in Fig. 3. The time-coefficient *n* [11] of the body-tied and the SOI FinFET with the SMS-method was 0.22~0.27, but the OTF-method shows an *n* value of 0.11 for both devices. The OTF-method eliminates the recovery-effects, thus showing non-recovered NBTI characteristics with the decreased time-coefficient [6,7]. The similar *n* resulting from the OTF-method for various device structures and oxide fields (E_{ox}) shows an identical degradation mechanism of NBTI, reaction-diffusion (R-D) model [6]. However, the E_{ox}-coefficient *m* shows no measurement method dependency while it does show device structure dependency, as seen in Fig. 4 [11]. The I_{SLin} degradation with various gate/drain pulse duties, the ratio of a stress pulse time to the total pulse time (monitor+stress time), are shown in Fig. 5 with a fixed stress bias of 3.3V to confirm the OTF-method. The independence of the gate/drain pulse duty shows that no recovery effects occurred during the OTF-method. The OTF-method uses a pulse duty of 70% in this work.

Fig. 6 shows the degradation of I_{SLin} on grounded body-tied FinFETs with various DC stress biases (V_{Stress}). The V_{Stress} increment induces additional holes at the Si/SiO2 interface and breaks more Si-H bonds. Fig. 7 and Fig. 8 show a gate length dependency of 2.6nm thin T_{ox} body-tied FinFETs with GPOX, and Fig. 9 shows a gate length dependency of 5.8nm thick T_{ox} SOI FinFETs with GPOX. The degradation by NBTI is reduced with the gate length decrement on thin gate oxide body-tied FinFETs, while no gate length dependency is found for thick gate oxide SOI FinFETs. Due to a fixed GPOX-affected gate length, the ΔL value in Fig. 1, an effective gate oxide thickness ($T_{ox,eff}$) increment with the gate length decrement is sensitive in the thin gate oxide device, but insensitive in the thick gate oxide device. Fig. 10 shows a gate length dependency of a 2.6nm T_{ox} body-tied FinFET on a device degradation with -0.2V V_{sub}. The decrement of NBTI degradation on a shorter gate length body-tied FinFET with a virtual-floating body results from the thin gate oxide thickness and GPOX.

Eq. 1 shows a revamped interface trap density (N_{it}) of 3D GPOX FinFET using a modified geometry-aware R-D model that considered 1D, 2D, and 3D diffusions of hydrogen at the Si/SiO_2 interface [12]. The $N_{H1x}^{(0)}$ value in the model represents the density of hydrogen at the interface in the x-axis with normal thickness of gate dielectric, $N_{H2y}^{(0)}$ represents the density of hydrogen in the y-axis on the GPOX affected region, and D_H represents the diffusion constant of hydrogen. Due to the thinner oxide thickness of the normal gate dielectric compared to that of GPOX area, $N_{H1}^{(0)}$ is larger than $N_{H2}^{(0)}$. Eq. 2 shows the difference of N_{it} with a different gate length ($L_{G1}>L_{G2}$) using Eq. 1. The geometry-dependent R-D model predicts a worse NBTI for a GPOX FinFET with a longer gate length.

Conclusions

Gate length dependency of NBTI was investigated on both body-tied and SOI FinFETs with GPOX using an OTF measurement method. The device degradation was reduced for shorter gate length devices due to the thicker effective gate oxide thickness by GPOX on a gate edge with a thin gate oxide thickness. A modified geometric considered R-D interface trap model showed worse NBTI behavior for longer L_G by GPOX. Using the GPOX process on a buried channel PMOS FinFET, enhanced off-state leakage performance as well as superior NBTI characteristics are achieved.

Acknowledgment

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References

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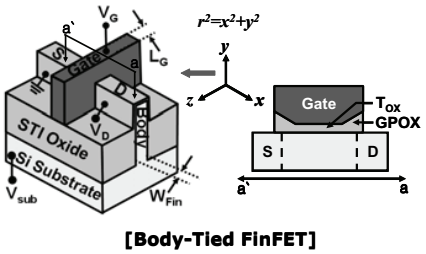

Fig. 1. The schematic of a PMOS body-tied FinFET with gate poly-silicon oxidation (GPOX) on the gate edge.

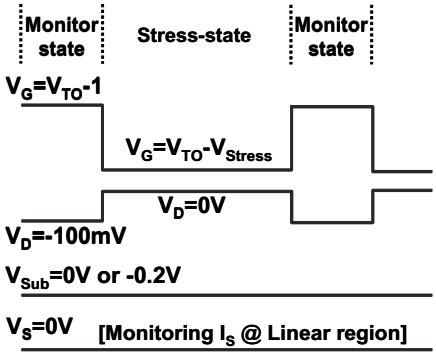

Fig. 2. Pulse-forms on the FinFET gate, drain, substrate, and source during the monitor- and stress-state using a parameter analyzer as well as a pulse generator.

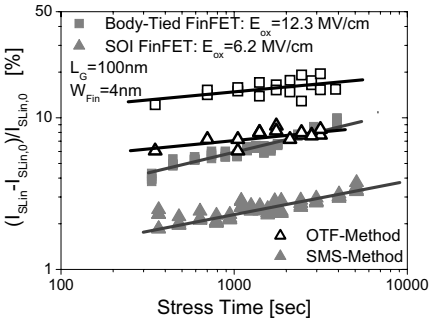

Fig. 3. The source linear-current degradation of a body-tied FinFET (E_{ox}=12.3MV/cm) and a SOI FinFET (E_{ox}=6.2MV/cm) with a stress time using the SMS- and OTF-methods.

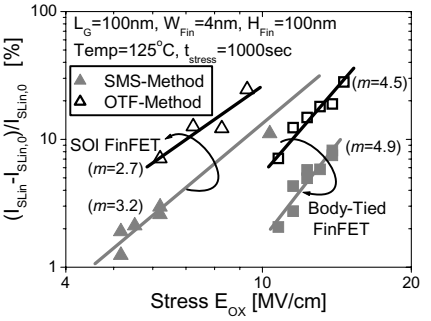

Fig. 4. The I_{SLin} degradation vs. stress E_{ox} with body-tied and SOI FinFETs at 100nm L_G and 4nm W_{Fin}. The E_{ox}-coefficient *m* shows no measurement method dependency, but shows a device structure dependency.

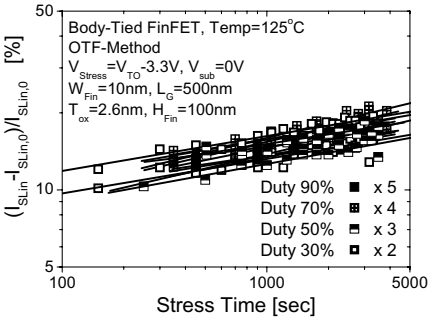

Fig. 5. The I_{SLin} degradation of body-tied FinFETs with various gate/drain pulse duties of 90, 70, 50, and 30% at a V_{stress} of 3.3V.

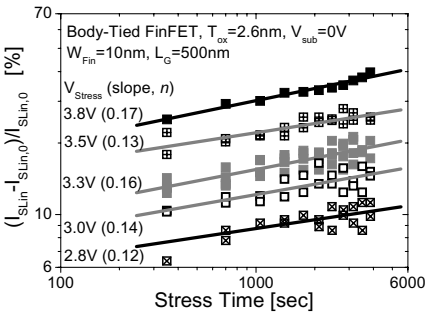

Fig. 6. The degradation of grounded body-tied FinFETs with various DC stress biases at 500nm L_G and 10nm W_{Fin}. A similar time-coefficient is extracted.

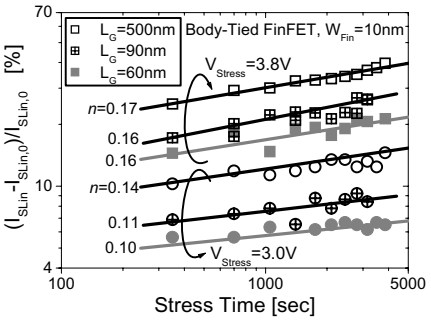

Fig. 7. The I_{SLin} degradation of 3.8V and 3.0V V_{Stress} body-tied FinFETs versus stress time for 60nm, 90nm, and 500nm L_G.

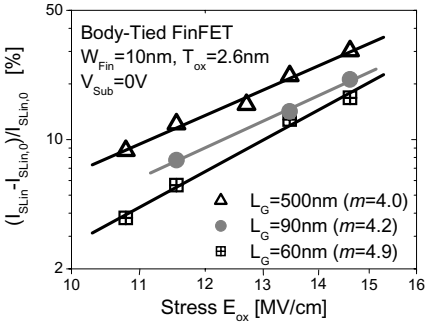

Fig. 8. The I_{SLin} degradation of 10nm W_{Fin} body-tied FinFETs versus stress E_{ox} with various L_G's. As the gate length decreases, the NBTI degradation is reduced due to the effects of the GPOX.

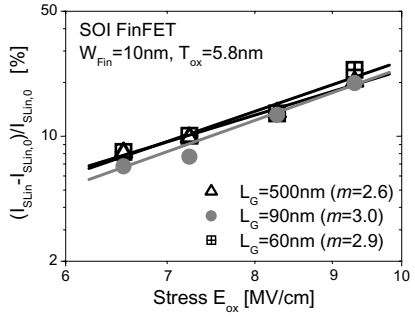

Fig. 9. The gate length dependency of a 5.8nm T_{ox} SOI FinFET with GPOX. The SOI FinFET shows no gate length dependency due to the thick gate oxide.

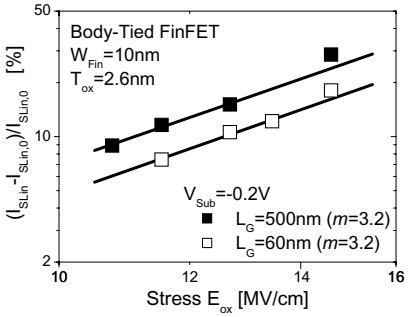

Fig. 10. The gate length dependency on the device degradation of a 2.6nm T_{ox} body-tied FinFET with -0.2V V_{sub} in a virtual-floating body device. The gate length dependency shows the effects of a thin gate oxide and GPOX.

$$N_{it}(t)= \left[\left(3N_{H1z}^{(0)}N_{H1y}^{(0)}\frac{\sqrt{D_H t}}{2}\right)+\left(\frac{2\pi}{12}N_{H1r}^{(0)}\sqrt{D_H t}\right)\right] \times\left[N_{H1x}^{(0)}-\frac{\Delta L}{L_G}\left(N_{H1x}^{(0)}-N_{H2x}^{(0)}\right)\right] +\frac{\pi}{6}\sqrt{D_H t}\left[\left(N_{H2r}^{(0)}\right)\left(N_{H2z}^{(0)}+2N_{H2y}^{(0)}\right)\right] +\frac{4}{6}\sqrt{D_H t}\left(N_{H1}^{(0)}\right)$$

Eq. 1. The interface trap density of a 3D GPOX FinFET structure using a modified geometry-aware R-D model [12].

$$N_{it,1}(t)-N_{it,2}(t)= \left[\left(N_{H1x}^{(0)}-N_{H2x}^{(0)}\right)\left(\frac{\Delta L}{L_{G2}}-\frac{\Delta L}{L_{G1}}\right)\right] \times\left[3N_{H1z}^{(0)}N_{H1y}^{(0)}+N_{H1r}^{(0)}\frac{\pi}{3}\right] \times\left[\frac{\sqrt{D_H t}}{2}\right]>0$$

$$\therefore N_{it,1}(t)>N_{it,2}(t)\ \ @\ L_{G1}>L_{G2}$$

Eq. 2. The interface trap density differences of GPOX FinFETs with gate lengths of L_{G1} and L_{G2}. The longer gate length device shows larger NBTI degradation.