NOVEL POLYSILICON THIN-FILM TRANSISTORS WITH NANOWIRE CHANNEL

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The novel polysilicon thin-film transistors with three-dimensional silicon nanowire channel have been fabricated and characterized. As the device dimension is scaled down, in the channel region of thin-film transistor, the number of polysilicon grain boundary defects will be dramatically reduced without additional recrystallization process. It can result in less scattering of carriers during transportation and eventually improve the performance of thin-film transistors. And the three-dimensional silicon nanowire channel with omega-gate has the better gate controllability and suppresses the short channel effects.

As a starting material of the polysilicon nanowire TFT, (100) bulk silicon wafer was used. After the 145nm thermal oxide (SiO_2) was grown as a buried oxide, a 20nm polysilicon film was deposited by LPCVD. The twin-well implantation was performed for CMOS devices. To achieve high resolution as well as high throughput, dual-photoresist process (e-beam lithography for nanometer scaled fin and gate, and KrF optical lithography for non-critical probing pad area) was used. After the silicon fin etching, a sacrificial oxide was grown and removed for forming a rectangle fin to rounded shape. During the subsequent etch of the sacrificial oxide, the buried oxide was over etched and undercut beneath the polysilicon channel was formed. This suspended nanowire channel can provide omega-gate structure. After the gate dielectric of 1.7nm SiO_2 was grown, a gate polysilicon was deposited and patterned by dual-photoresist process and anisotropic etch. The gate spacer was conventionally formed, then As and BF_2 were implanted for source/drain of NMOS and PMOS respectively.

Fabricated devices have length of 80~100nm, width of 10~20nm. The transistor switching characteristics are remarkably improved. ON-state current which is normalized by arounded channel perimeter is 28~40uA/um. Normalized OFF-state leakage current is $2.7X10^{-10}$A/um. The ON/OFF current ratio is $1.12X10^{5}$ and the device shows very sharp subthreshold slope (SS=71mV/dec). Fabricated device shows a small drain induced barrier lowering (DIBL=53mV/V).