A Nanowire Transistor for High Performance Logic and Terabit Non-Volatile Memory Devices

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Abstract

A silicon nanowire-FET (SiNAWI-FET) for high performance logic device with consideration of current direction effects and terabit non-volatile memory (NVM) device using an 8nm SiNAWI-NVM with oxide/nitride/oxide (ONO) and omega-gate structure is reported for the first time. N- and P-channel SiNAWI-FET showed the highest driving current on (110)/<110> crystal orientation without device rotation, whereas most 3-dimensional NMOS report higher driving current on 45° device rotation rather than 0°. Utilizing an 7nm spherical nanowire on the 8nm SiNAWI-NVM with ONO structure, 1.7V V_T-window was achieved from 12V/80μsec program conditions with retention enhancement.

Introduction

In the ultimately scaled nano-scale regime, a multiple-gate with a nanowire channel shows high robustness on short-channel immunity and superior scalability using conventional processes [1-7]. And the strength was certified by fabrication of a sub-5nm NMOS all-around gate (AAG) FinFET [5]. Due to the high driving current, low drain leakage, and scalability of SiNAWI-FET with strong gate controllability, it has potential to be used in a high performance logic and terabit non-volatile memory devices.

When a silicon bulk channel is changed to nanowire, band structure considered carrier transport on driving current with different channel direction becomes dominant [8-10]. And to fabricate sub-10nm NVM using a non-scalable ONO structure, silicon nanowire channel with multiple-gate structure are suitable [11-15]. In this paper, CMOS SiNAWI-FETs with channel direction effects are reported for the first time through experiment data. And this work primarily focuses on scalability and feasibility of terabit non-volatile memory using an 8nm SiNAWI-NVM with wide V_T window and prolonged retention characteristics.

Fabrication

Process flows of the CMOS SiNAWI-FET and SiNAWI-NVM are illustrated in Fig. 1. The sequences are similar to those of a sub-5nm NMOS AAG FinFET with 3nm fin width [5], except for following differences: (a) n-well implantation was performed on a PMOS SiNAWI-FET after silicon body thinning. (b) 2nm thermal oxide and undoped 30nm polysilicon were grown and deposited for the CMOS SiNAWI-FET and n^+/p^+ gate implantation was performed. (c) A control oxide layer, nitride trap layer, blocking oxide layer, and 30nm in-situ n^+ polysilicon were grown and deposited to fabricate SiNAWI-NVM. (d) Arsenic and BF_2 ions were used as source/drain implantation impurities. TEM cross-sectional views of the SiNAWI-NVM with an 8nm (L_G) omega-shaped gate on a 7/10.5nm (W_{NW})/(H_{NW}) spherical silicon nanowire channel with 3.8/6.4/5.1nm ONO-structure are shown in Fig. 3. SEM top-views of the 8nm gate on the silicon channel with 2nm SiO_2 and 45° rotated SiNAWI-FET are shown in Fig. 4.

Results and Discussion

A. CMOS SiNAWI-FET with Orientation Effects

Normalized electrical characterizations of a 55nm CMOS AAG SiNAWI-FET with 5nm W_{NW} are shown in Fig. 4. The lower PMOS driving current influences of boron penetration from the p^+ gate as well as poly depletion effects. The impact of W_{NW} on device V_T is shown in Fig. 5. The V_T shift of CMOS SiNAWI-FET with narrow W_{NW} is increased by quantum confinement effects, and the analytical model shows good agreement with the measured data [5,6,15]. Fig. 6 shows the channel direction effects on the CMOS SiNAWI-FET with rotated channel angles from 0° to 75° for NMOS and 0° to 45° for PMOS, as shown in the inset of Fig. 3 and Fig. 6(b). Both N- and P-channel SiNAWI-FET show higher driving current in the (110)/<110> current direction with 0° device rotation than in the (010)/<100> current direction with 45° rotation, due to a lighter transport effective mass on the silicon nanowire channel [8,10]. The results correspond well with full-band simulation data from ref. [8], but contradict findings from ref [9]. For the SiNAWI-FET, both NMOS and PMOS show the highest driving current on 0° device rotation without complicated layout modification, i.e. NMOS 45° rotation.

B. SiNAWI-NVM with ONO-Structure

The I_D-V_G hysteresis curves of the 8nm SiNAWI-NVM with 7nm W_{NW} for various programs and erase voltages are shown in Fig. 7 and Fig. 8. The acceptable electrical characteristics of the 8nm NVM with thick ONO-structure are influence of the omega-shaped gate structure by the superior gate controllability. Despite the ultimately scaled device size, the wide hysteresis can provide multi-level NVM operation. Fig. 9 shows program/erase (P/E) characteristics of the 8nm memory cell with a 1.7V threshold voltage shift (ΔV_T) for 12V/80μsec program condition and ΔV_T saturation from erase condition of -12V/1msec [13]. The reduced P/E voltage with fast P/E time is due to the effects of the narrow silicon nanowire structure, as shown in Fig. 10. The ΔV_T enhancement with narrow W_{NW} is due to an effective energy bandgap widening of the silicon channel by a quantum confinement effect, which induces a higher tunneling coefficient from the channel to the storage nodes [16-18]. This phenomenon also affects the retention characteristics of 38nm SiNAWI-NVM with various W_{NW}, as shown in Fig. 11. As the W_{NW} is reduced to 7nm, the 10-year charge loss from the extrapolated retention characteristics is radically decreased to 7%. The improvement on the extremely narrow W_{NW} is mainly caused by the low tunneling possibility of the stored charges in the reverse direction at the program operation and the spherical silicon nanowire without corner effects. The performances of the SiNAWI-NVM are comparable to published values of 3-dimensional ONO-NVM, due to the narrow spherical silicon nanowire and omega-gate structure.

Conclusions

The smallest memory cells of 8nm SiNAWI-NVM with ONO-structure and CMOS SiNAWI-FET with AAG-structure were fabricated. Owing to the nature of the silicon nanowire channel, the CMOS SiNAWI-FET showed the highest driving current in the (110)/<110> channel direction without device rotation for the first time using experimental data. The 8nm SiNAWI-NVM with enhanced V_T-window and retention properties shows feasibility of terabit non-volatile memory using a nanowire structure.

References

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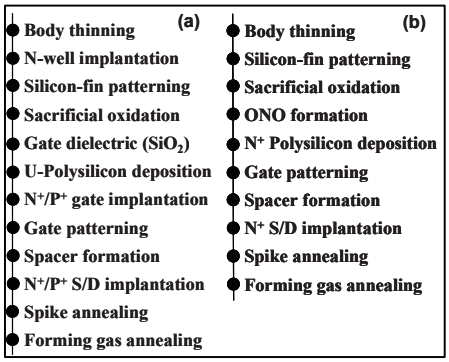


Fig. 1. Process flows of (a) CMOS SiNAWI-FET and (b) SiNAWI-NVM with ONO.

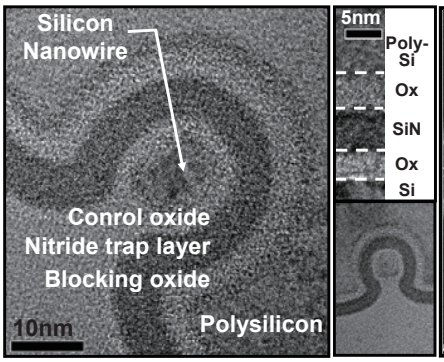


Fig. 2. TEM images of 7/10.5nm (W_{NW}/H_{NW}) spherical silicon nanowire with ONO.

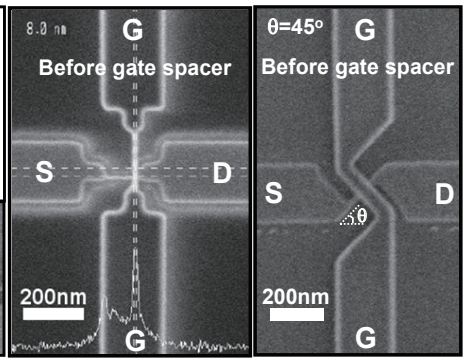


Fig. 3. SEM images of 8nm omega-gate on silicon-fin with 2nm SiO_2 and 45° rotated channel device.

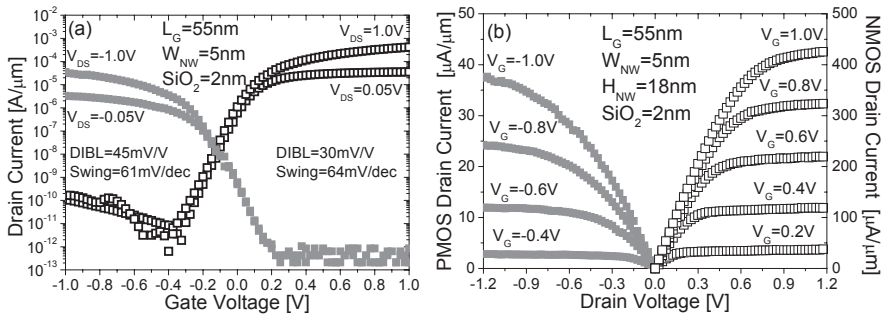


Fig. 4. Normalized (a) I_D-V_G and (b) I_D-V_D characteristics of CMOS all-around gate SiNAWI-FET with L_G=55nm, W_{NW}=5nm, H_{NW}=18nm, and SiO_2=2.0nm.

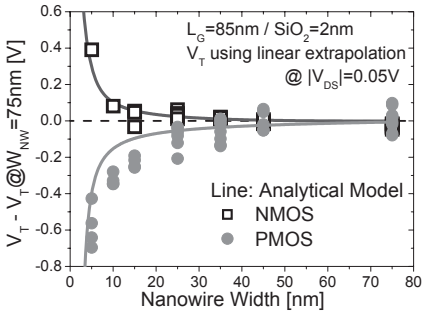


Fig. 5. ΔV_T vs. W_{NW} on NMOS and PMOS SiNAWI-FETs with analytical model [5].

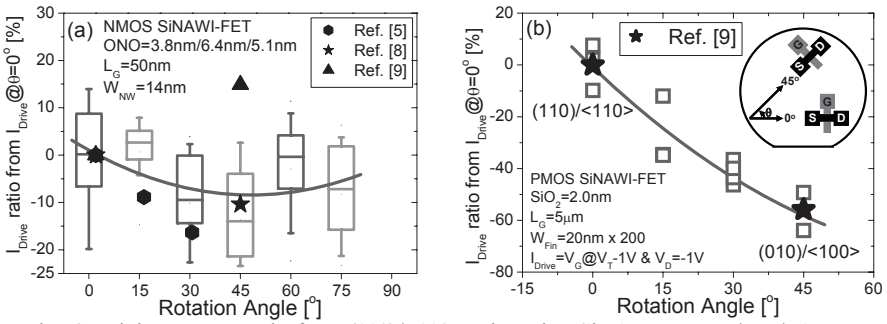


Fig. 6. Driving current ratio from (110)/<110> orientation SiNAWI-FET at $|V_{DD}|$=1V versus device channel rotation angle at (a) 50nm NMOS and (b) 5μm PMOS.

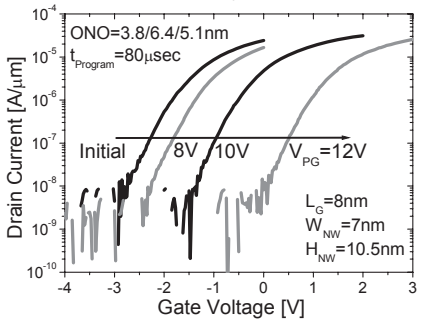


Fig. 7. I_D-V_G curves with various program voltages on 8nm SiNAWI-NVM.

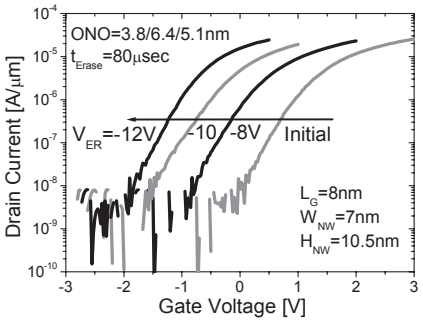
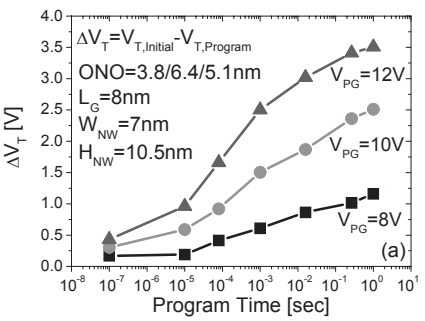


Fig. 8. I_D-V_G curves with various erase voltages on 8nm SiNAWI-NVM.



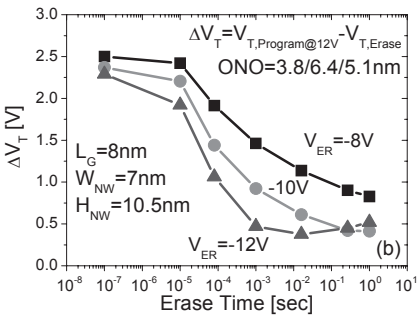


Fig. 9. Transient characteristics of 8nm SiNAWI-NVM with ONO-structure (a) program bias of 8, 10, 12V and (b) erase bias of -8V, -10V, -12V with ΔV_T saturation.

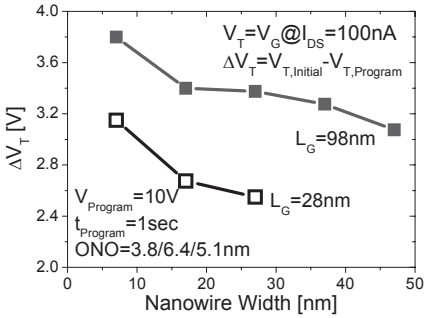


Fig. 10. ΔV_T dependence on nanowire width on SiNAWI-NVM with fixed L_G.

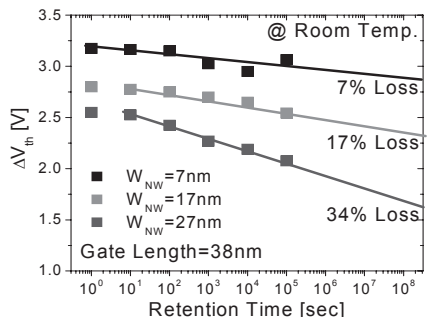


Fig. 11. Retention characteristics and 10-year charge loss on 38nm device with various W_{Fin}.

Acknowledgment

The authors would like to thank Dr. Hee Chul Lee for managerial support from the Korean National Nanofab Center, and Kanghoon Jeon for useful discussions.