Retention Mechanism in Double-Gate 1T Capacitorless DRAM by Using PiFET Structure

Dong-il Bae, Sungho Kim, and Yang-Kyu Choi
School of Electrical & Computer Science, Korea Advanced Institute of Science and Technology,
373-1 Guseong-dong Yuseong-gu, Daejeon, 305-701, KOREA Phone : 82-42-869-5477 Fax:82-42-869-8565 E-mail:equal72@nobelab.kaist.ac.kr

Introduction

Since a capacitorless 1 transistor (1T) DRAM idea was proposed [1] on a partially depleted SOI, various kinds of 1T DRAM concept have been proposed. To suppress the degradation of the retention caused by a trap-assisted tunneling and improve the control of short-channel effects, a double-gate type 1T DRAM [2] formed on a fully depleted SOI was already studied. For the process compatibility with a bulk wafer, a new kind of 1T DRAM formed on a bulk wafer was also previously presented [3]. There were another previous works which figured out that a major reason of the retention degradation is heat dissipation and '0' state retention is more vulnerable [4].

In this work, we compared a PiFET 1T DRAM [5] with a SOI 1T DRAM to analyze the dominant factor of retention degradation. A PiFET structure, especially PUC (PiOX Under Channel) structure, can act as 1T DRAM by applying a negative back bias. It shows lower electrical field and more process compatibility with the bulk silicon than the conventional SOI 1T DRAM. By using this structure, we investigated the enhancement method of the retention time.

Simulation

Fig.1 is the conventional SOI 1T DRAM structure and **Fig.2** is the PiFET 1T DRAM structure. Electrical isolation from p-well is made by isolated insulator (buried oxide: PiOX) at the partial bottom of the channel and a negative bias of substrate to source/drain (S/D). Thus, all structures used in this work are double-gate. It also shows floating body cell behavior. Advantages of the PiFET structure are in lower electrical field near S/D, and it will improve the retention characteristic. It also provides wide design flexibility in process parameters such as an overlap length of PiOX, a thickness of PiOX, a material of PiOX, and a substrate doping, etc. By comparing with the conventional DG FDSOI 1T DRAM, a retention mechanism proposed in this paper can be verified.

To simulate the retention time, we calculated the accumulated hole charges. By integrating the hole density at 1nm above of the PiOX, accumulated hole charges are calculated as shown in **Fig. 1, 2**. By using transient simulation mode, the retention time is represented with variation of accumulated hole charges as time varies.

Mechanism of Retention Degradation

The conventional retention graph reported in various papers and newly proposed degradation mechanism is represented at **Fig.3**. There are two kinds of important factors which strongly affect the 1T DRAM's retention time. The first one is initial accumulated hole charges. More initial hole charges make the larger difference between '0' and '1' state. It means that threshold voltage difference or driving current difference is large. The other factor is the position of equilibrium state. Retention degradation of '1' state is caused by recombination of accumulated hole charges. Off-state leakage current and potential barrier lowering are major causes of the recombination. Degradation of '0' retention is caused by generation of hole charges. Major generation factors are BTBT, thermal generation, and GIDL effect of the back gate. But, BTBT can happen only under disturb condition. So it is not a major degradation factor. Beyond a critical time, even though it is measured or simulated separately, generation and recombination ratio will be the same, and it makes equilibrium state. This implies that '0' and '1' retention cannot be improved separately, and the position of equilibrium state decides the retention characteristics.

Results and Discussion

The first degradation factor is an electrical field at body to source. **Fig.4** shows that PiFET 1T DRAM shows lower electrical field than the conventional 1T DRAM because of potential lowering by substrate to S/D bias. Lowered electrical field causes lower thermal generation and results in good '0' retention as shown in **Fig.5**. But the PiFET structure can cause the impact ionization near substrate to S/D. It can make the hole generation and degrade the '0' retention as shown in **Fig.6**. To suppress the hole generation and to improve the retention, junction optimization is demanded.

GIDL effect of back gate to drain also plays an important role in retention. If higher back gate bias is applied, it causes higher GIDL and degrades the '0' retention as shown in **Fig.7**. High temperature also degrades the '0' retention without degradation of retention factor due to thermal generation as shown in **Fig.8**. **Fig.9** shows structural effect. PiFET and FDSOI show the same degradation ratio caused by GIDL effect. There is no degradation at PiFET structure as temperature increase, but FDSOI structure shows severe degradation.

Fig.10 shows the doping effect. As the doping concentration increases, programmed hole charge quantity increases. But it can increase the GIDL effect as well and cause high electric field between body to source. Consequently larger retention factor is made. This means that '0' retention is degraded.

Fig.11 shows the BOX thickness effect. As the BOX thickens, the GIDL effect causing the improvement of '0' retention decreases. Therefore the retention factor will decrease. But thick BOX results in small body capacitance and causes small initial hole charges. It can degrade '1' state retention. **Fig.12** shows the BOX material effect. If high-k dielectric is adopted, larger hole charge and higher electric field is generated. It leads to degradation of '1' retention. But the same dielectric thickness didn't affect at '0' retention.

Conclusions

The mechanism of the retention degradation in DG capacitorless 1T DRAM is investigated by using PiFET structure. It showed low electrical field and good temperature immunity. Moreover, proposed degradation model showed good match with simulation result.

References

[1] H. Wann et al., IEDM Tech. Dig., 1993, p645, [2] C. Kuo et al., IEDM Tech. Dig., 2002, p843, [3] R. Ranica et al., Symp. VLSI Tech. Dig., 2004, p128, [4] R. Ranica et al., IEDM Tech. Dig., 2004, p277, [5] KH. Yeo et al., 2004, EDL, p387.

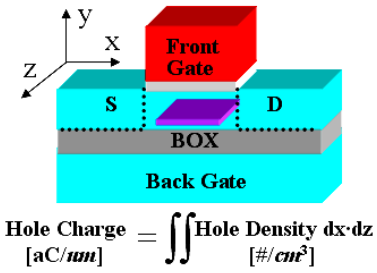


Fig.1 FDSOI 1T DRAM structure.

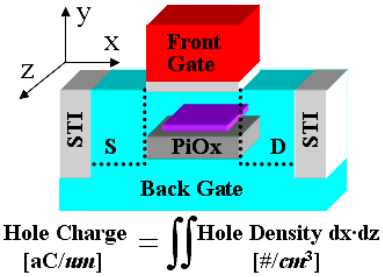


Fig.2 PiFET 1T DRAM structure

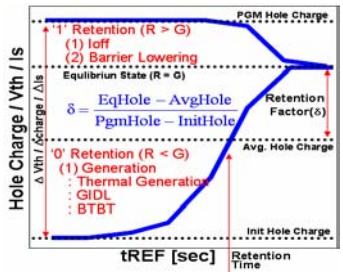


Fig.3 Conventional 1T DRAM retention graph and degradation mechanism.

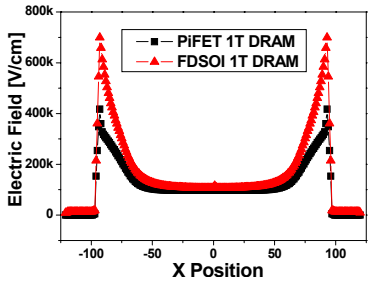


Fig.4 PiFET 1T DRAM shows lower electrical field than conventional SOI 1T DRAM.

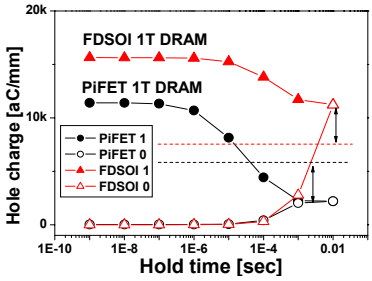
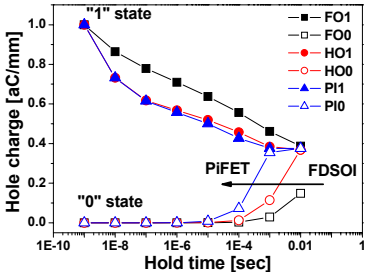


Fig.5 PiFET 1T DRAM shows better '0' retention than FDSOI 1T DRAM.



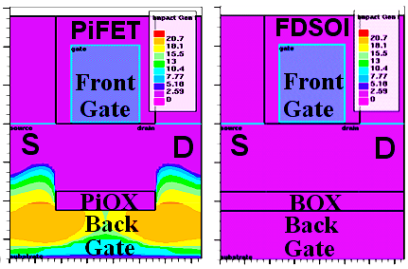


Fig.6. (a) Normalized retention at non-optimized structure. (b) Degradation induced by impact ionization near back gate to drain/source.

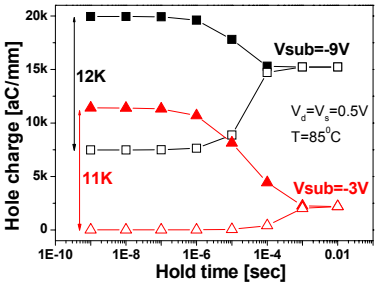


Fig.7 Higher Back Gate bias induce higher GIDL and degradation of '0' retention. Retention factor degradation is observed.

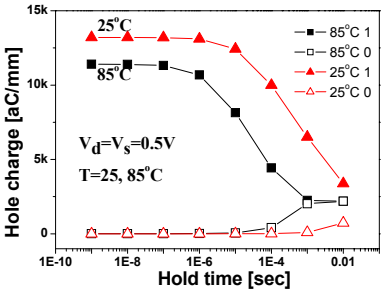


Fig.8 High temperature shows short retention time by thermal generation. Degradation of retention factor is not observed.

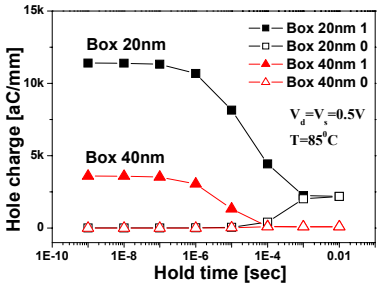
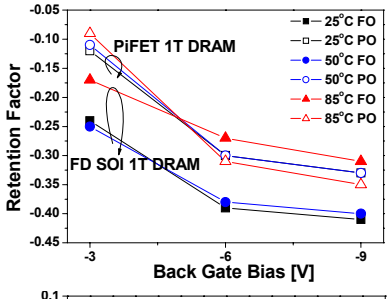


Fig.11 "0" Retention degradation by BOX Thickness.



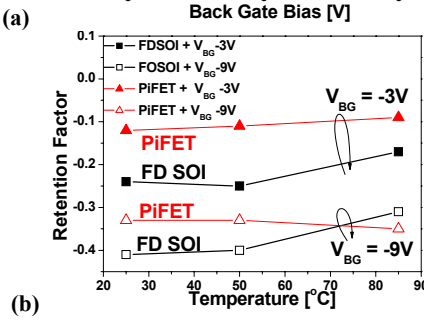
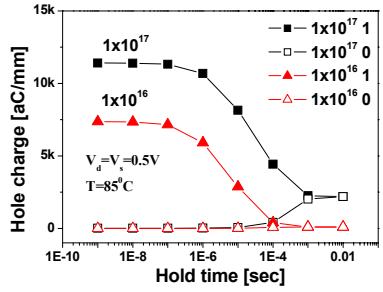


Fig.9 Retention Factor by Temperature and GIDL effect. (a) Back Bias Effect (GIDL) (b) Temperature effect



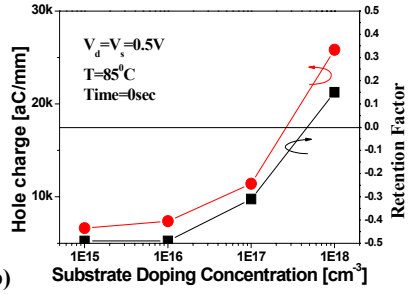


Fig.10 "0" Retention degradation by Doping Concentration. (a)Retention (b) Programmed hole charge and Retention Factor

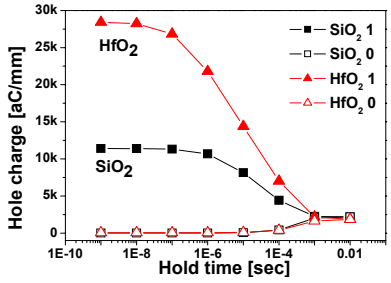


Fig.12 "1" Retention degradation by BOX material.