3 차원 수직형 나노쉘 전면 게이트 구조의 전계효과트랜지스터

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요약 극한의 소자 스케일링을 위한 새로운 3 차원 수직형 나노쉘 전면게이트 구조의 전계효과트랜지스터를 제안하였다. 제안된 수직형 나노쉘 구조는 증착된 다결정실리콘 박막과 고상결정화 (SPC) 공정을 이용하여 형성된 실리콘 박막 바디와 전기적으로 독립된 내부 게이트를 통하여 구현할 수 있다. 3 차원 실바코 시뮬레이션 툴을 이용하여 수직형 나노쉘로 대표되는 더블 전면게이트 구조와 나노와이어로 대표되는 싱글 전면게이트 구조를 비교하여 소자의 스케일링 다운시 가장 큰 문제가 되는 단채널 효과 (SCE) 측면에서의 본 구조의 장점을 제시하였다. 그리고 독립적인 내부 게이트의 바이스를 여러 방법으로 변화시키면서 문턱전압 변화를 비롯한 전기적인 특성과 함께 저전력 트랜지스터로의 이용 가능성을 고찰하였다.

키워드 나노쉘 구조, 전면게이트, 고상결정화, 단채널 효과

3-Dimensional Vertically Integrated Nano-Shell All-Around-Gate MOSFET

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Abstract This paper reports a novel 3-dimensional vertical nano-shell all-around-gate MOSFET for ultimate device scaling. The vertical nano-shell structure can be realized by introduction of a silicon thin-body formed by chemical vapor deposition (CVD) of poly-silicon and subsequent solid phase crystallization (SPC) as well as incorporation of an electrically independent inner-gate. It was verified that the vertical nano-shell MOSFET offers immunity to short-channel effects through a comparison of device performances between a nano-shell structure (double all-around-gate) and a nano-wire structure (single all-around-gate) with the aid of a SILVACO® 3-D simulator. With diverse modulations of the bias from the independently operated inner gate, the electrical characteristics of the MOSFET and the feasibility of application to a low-power transistor are investigated.

Keyword Nano-shell structure, All-around-gate, Solid phase crystallization (SPC), Short-channel effect (SCE)

1. Introduction

Recently, new conceptual devices such as non-planar multi-gate devices have been reported for nano-CMOS, attracting much attention due to their excellent immunity to short-channel effects and high gate controllability [1]-[6]. In particular, a nano-wire device has been considered as an ultimate 3-dimensional (3-D) device structure. Specific features of the 3-D device include an ultra-thin body (channel) and a multiple-gate partially or fully surrounding the channel. In terms of fabrication complexity, however, controllability of uniform diameter and difficulties in realizing short-gate length pose obstacles to the practical application of this nano-wire device. One of the primary issues in such ultra-thin body devices is the adjustment of the threshold voltage (V_T), because the bulk charges to tune the threshold voltage significantly decrease due to the nature of the ultra-thin body. Alternatively, tuning of the threshold voltage can be achieved by gate

workfunction engineering and separable gates such as a top- / bottom-gate or outer- / inner-gate. In addition, tunable threshold voltage characteristics are important to achieve low current for low power consumption devices.

In this work, employing solid phase crystallization of a deposited silicon film formed by CVD and separated outer- and inner-gates fully surrounding a shell-shaped channel, we demonstrate high on-state and low subthreshold current properties. High ratio of on-current to off-current can be realized by an all-around-gate (AAG) structure and a tunable threshold voltage characteristic in a vertically integrated nano-shell MOS field effect transistor. A comparison of device performances between the nano-shell structure (separated double AAG) and the nano-wire structure (tied single AAG) with the aid of a 3-D simulator verifies that the vertical nano-shell MOSFET provides immunity to short-channel effects. With diverse modulations of the bias from the separated gate, electrical characteristics of nano-shell device as well as its feasibility of application to a low-power consumption transistor are investigated.

2. Fabrication Process

Fig. 1 shows the process flow to fabricate the vertical nano-shell AAG MOSFET. First, a silicon substrate is oxidized for a bottom inter layer dielectric (ILD) layer to isolate each electrode. TiN (workfunction = 4.8eV) is deposited for the outer-gate material, and another oxide is sequentially deposited by CVD for a top ILD, as shown in Fig. 1(a). In this vertical structure, the deposited TiN thickness for the outer-gate material automatically determines the physical gate length, which can be a sub-lithographic size beyond the resolution limit of lithography. Next, a trench hole is formed by anisotropic dry etching of the top ILD, deposited TiN, and the bottom ILD to create a channel (Fig. 1(a)). Ion implantation is conducted to make a shallow source region on the silicon substrate through the hole (Fig. 1(b)). A conformal outer gate dielectric is formed along the hole (Fig. 1(c)). This gate dielectric is subsequently removed both from the silicon substrate and the top ILD by a blanket etch-back process. As a result, a sidewall profile of the gate dielectric can be made (Fig. 1(d)). The subsequent poly-silicon channel will thereby be electrically connected to the source region on the silicon substrate and along the hole. Amorphous or polycrystalline silicon to become a shell-shaped channel, is then deposited on the exposed substrate (Fig. 1(e)). After this deposition, a solid phase crystallization (SPC) process is applied and the nano-shell shaped amorphous or polycrystalline silicon channel is re-crystallized in a desired region.

Solid phase crystallization (SPC) is a commonly employed method to re-crystallize amorphous or polycrystalline silicon [7]. If high temperature annealing is applied to the amorphous or polycrystalline silicon over a long time, regular single crystals or large-sized grains will grow via phase transformation. According to previous works [8][9], grain size larger than the channel area can be realized through optimization of the temperature and annealing time.

Finally, an inner-gate dielectric is formed, and an inner gate material is subsequently deposited on the crystallized channel. This inner gate is defined by another lithography process for self-aligned drain formation (Fig. 1(f)). The inner gate can play a role as a mask during the subsequent ion implantation step to make the drain electrode.

3. Simulation results

Fig. 2 shows a schematic of the simulated vertical nano-shell AAG MOSFET. The simulation is performed under the assumption that all body regions of the channel are completely re-crystallized through the SPC process. The vertical nano-shell AAG MOSFET has independent double gate structures and thus the same or different biases can be applied simultaneously to the outer-gate (G1) and inner-gate (G2).

Oxide thickness (T_{ox}) for both the outer- and inner-gate dielectric is 2nm, body doping concentration (N_{Body}) is $10^{17}/cm^3$, and source/drain doping concentration (N_D) is $10^{20}/cm^3$. Gate length (L_G) is varied from 20nm to 40nm, and body thickness (T_{Body}) is varied from 5nm to 10nm. A nominal structure for the simulation has 30nm gate length, 5nm body thickness, and a TiN outer- / inner-gate.

3.1 Electrical characteristics

Fig. 3 shows typical electrical characteristics of the vertical nano-shell AAG MOSFET at the synchronized mode operation. The synchronized operation implies that the outer-gate and inner-gate are simultaneously varied within the specific range of the gate biases. Despite the short-gate length of 30nm, the vertical nano-shell MOSFET exhibits a near ideal subthreshold swing (S.S., ~60mV/dec) and a low level of drain induced barrier lowering (DIBL, ~20mV/V). These characteristics are due to the nature of the double AAG structure, which maximizes the gate controllability over the channel potential electrostatically.

Fig. 4 presents a comparison of V_T and S.S. in the nano-wire (single AAG) and the nano-shell FET (double AAG) structure

for various gate lengths. Due to the strengths of the double AAG, the nano-shell structure exhibits smaller V_t roll-off and S.S. It can be deduced that the nano-shell structure is more advantageous than the nano-wire for ultimately scaled devices.

Fig. 5 shows the inverted electron density across the nano-wire and the nano-shell, which are compared at the on-state (V_g=1V and V_d=1V) and subthreshold state (V_g=0.3V and V_d=1V), respectively, at the same body thickness, 5nm. A corner effect at the edges of the body is also observed. As shown in Fig. 5(a), the electron density of the nano-wire near the interface is high enough for channel inversion. As predicted, the electron density becomes lower toward the core region of the nano-wire. It is worth noting that the cross-section of the nano-shell for the on-state shows higher electron density at most regions except for the corner of the body, as shown in Fig. 5(c). This phenomenon can be alleviated by forming a round-shaped hole in the lithography process to define the hole as shown in Fig. 1(a). The nano-shell also shows better subthreshold characteristics than the nano-wire. This results in a low leakage current in the vertical nano-shell MOSFET. This feature is advantageous with respect to the realization of a low power (static power) consumption device for mobile applications.

Fig. 6 shows the body thickness modulation effect on V_T roll-off and S.S.. If the body thickness is decreased, a volume inversion occurs easily by increment of gate controllability, and thus immunity to short-channel effects is increased by a reduction of the body thickness. In the proposed nano-shell device structure, a thin and uniform channel is easily formed through the thin film deposited by CVD. Notably, high-resolution lithography tools are not required to make the nano-wire or the nano-shell, because the body (channel) thickness is controlled by the deposited film thickness.

3.2 Low-power device application

Fig. 7 compares the electrical characteristics at the synchronized mode operation between the same (V_{G2}=V_{G1}) and different initial gate biases. Channel inversion occurs in all channel areas simultaneously at the same gate bias while it occurs in certain regions of the channel area with different initial gate biases. The V_T shift rate can be expressed as

$$\gamma = -\delta V_T / \delta V_{g2}$$

. For present vertical nano-shell structure at the synchronized mode the V_T shift rate (γ) is approximately 0.6 at the region which initial bias difference (V_{G2}-V_{G1}) is positive. Also, this structure shows degraded S.S. with different initial gate biases. Fig. 8 shows the electrical characteristic at the static mode of the inner-gate bias (fixed gate bias of V_{G2}). By increasing the inner-gate bias toward positive, γ becomes higher but S.S. is degraded rapidly at V_{G2}>0.4V referring to inset in Fig. 8. However, as the inner-gate bias is increased toward negative, γ becomes smaller and is eventually saturated at V_{G2}=-0.8V. This indicates that when positive bias over 0.4V is applied, core region near inner–gate changes from depletion to inversion state by increasing $V_{G2,}$ which results in the rapid changing in the S.S. and V_T [10]. Meanwhile, when negative bias is applied, the surface state of the inner-gate side is in the accumulation state and is pinned regardless of the inner-gate biases. Thus, the drain current no longer shifts with modulation of the gate bias [11].

4. Conclusion

It has been demonstrated that the vertical nano-shell AAG MOSFET shows better immunity to the short-channel effects than the nano-wire structure in comparison. Besides the suppressed short-channel effects, the nano-shell AAG MOSFET has provided high performance property, which is close to ideal characteristic and tunable threshold voltage characteristic with the aid of separated double gate structure. Based on these improved performance, low power consumption device is feasible by non-synchronized gate operation modes as well.

Acknowledgement

This research is partially sponsored by Samsung Electronics Co. Ltd.

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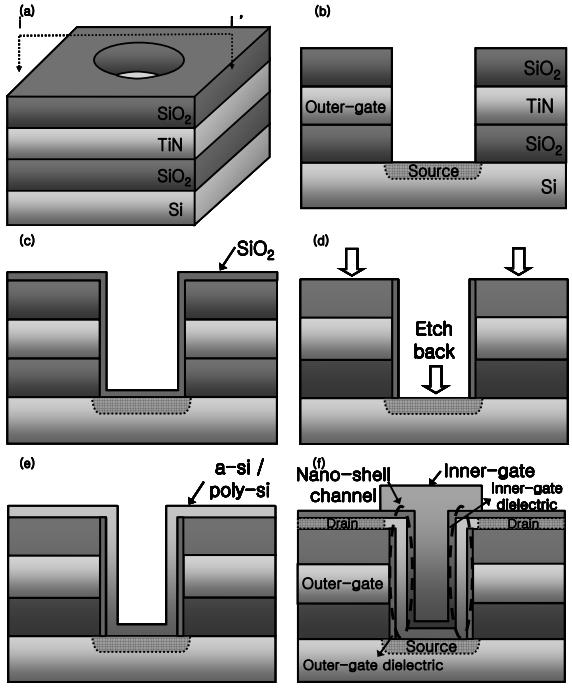


Fig. 1. Process flow of the vertical nano-shell AAG MOSFET.

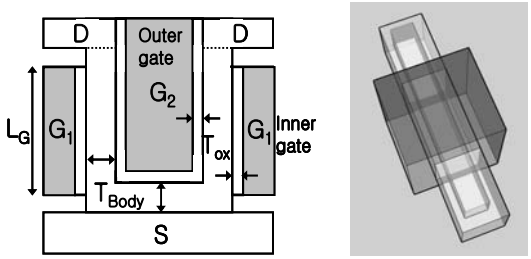


Fig. 2. Schematic of the simulated vertical nano-shell AAG MOSFET.

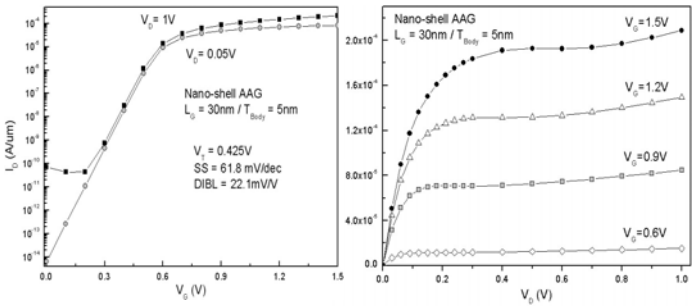


Fig. 3. I_D-V_G and I_D-V_D characteristics of the vertical nano-shell AAG MOSFET (at the synchronized mode operation).

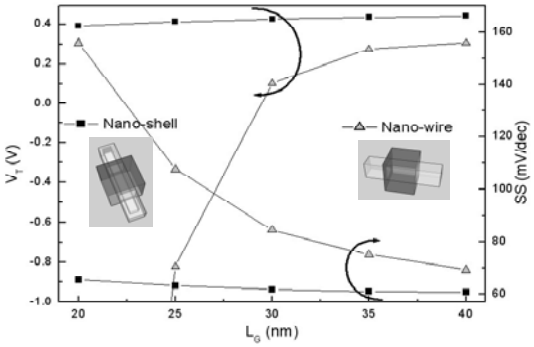
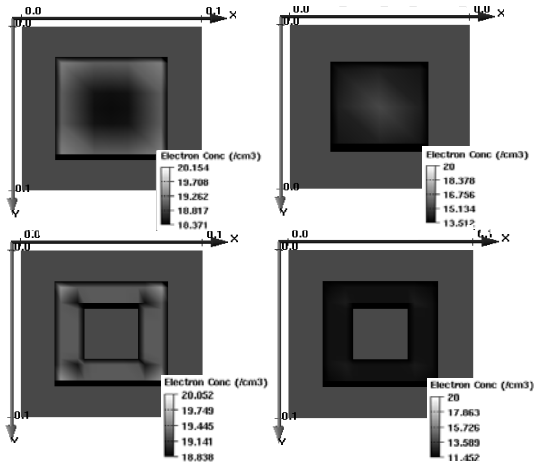


Fig. 4. V_T roll-off and S.S. versus L_G in the nano-wire (Single AAG) and nano-shell FET (Double AAG).



(a) Nano-wire at V_G =1V / V_D=1V (b) Nano-wire at V_G=0.3V / V_D=1V
(c) Nano-shell at V_G =1V / V_D=1V (d) Nano-shell at V_G=0.3V / V_D=1V

Fig. 5. Electron density across the nano-wire and the nano-shell.

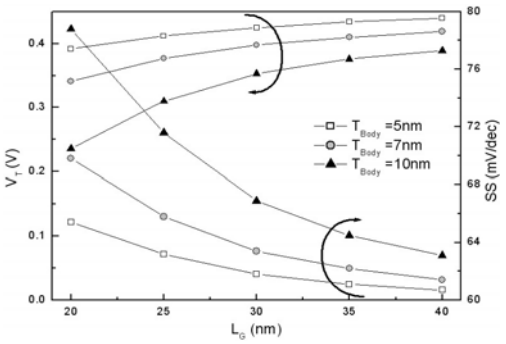


Fig. 6. Body thickness modulation effect on V_T-roll off and S.S.

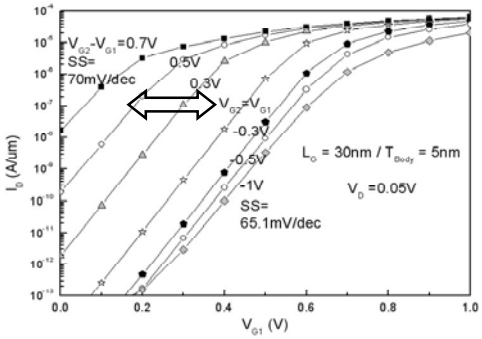


Fig. 7. Electrical characteristic at the synchronized mode operation with various bias effects. (V_{G1} and V_{G2} start from the same or the different initial biases and varies simultaneously) .

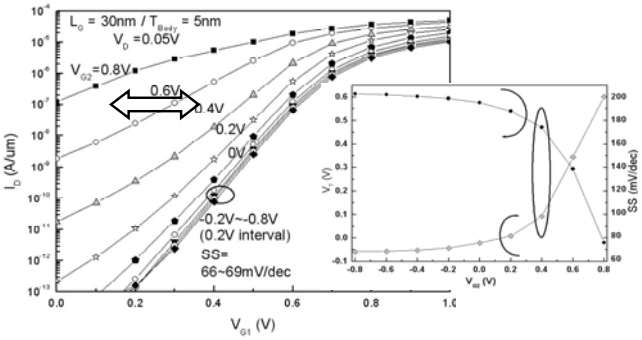


Fig. 8. Electrical characteristic at the static mode (V_{G1} varies with fixed V_{G2} bias). The inset shows V_T and S.S. as a function of V_{G2}.