Extremely Scaled 3-Dimensional Multiple Gate Technologies for Terabit Era

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As the device is scale down to a nano-scale regime, a channel potential controllability by a gate is reduced due to a high lateral electric field penetration from a drain, known as short-channel effects (SCEs). 3-dimensional (3D) multiple gate structures with a thin body were proposed to suppress SCEs by improvement of gate field effects on channel electrostatics.

When a channel length is down to 10nm in the thin-body devices, punchthrough characteristics, parasitic source/drain (S/D) series resistance, gate misalignment, and hot-carrier injection (HCI) effects become crucial issues for aggressive scaling. To avoid the punchthrough leakage, high dose halo implantation or underlapped S/D to gate structure may be required, but it results in reducing on-state current. The punchthrough leakage is significantly suppressed by utilizing the thin-body which is surrounded by the multiple gates without sacrifice of the on-state current. To understand the effects of S/D series resistance and gate misalignment, 3D mixed-mode FO4 circuit simulation was performed for the first time. The gate delay performance of a floating body SOI FinFET is better than a body-tied bulk FinFET due to a small diffusion capacitance. The HCI reliability is received attention by a slow scaling speed of operation voltage against a gate oxide thickness. As the body thickness is reduced, thinner body shows better immunity to the hot carrier stress because of the increased series resistance, which also causes reduction of the on-state current.

The sub-5nm all-around gate structure is proposed and fabricated for the extremely scaled devices with better punchthrough performances and lower off-state leakage current. And a floating body FinFET structure was used to increase the gate delay performance. The extremely narrowed 3nm body thickness (fin width) was used to improve SCEs and HCI reliability. The n-channel all-around gate FinFET with sub-5nm gate length, 1.4nm HfO_2 gate dielectric, and 3nm fin width shows 497 μA/μm on-state current at $V_G=V_D=1.0V$. This results show a feasibility to continue the Moore's law to be alive beyond the sub-5nm.