

Nonvolatile Memory Characteristics of NMOSFET with Silver Nanocrystals Synthesized by Thermal Decomposition Process

Seong-Wan Ryu*, Chan Bin Mo[†], Soon Hyung Hong[†] and Yang-Kyu Choi*

*Department of Electrical Engineering and Computer Sciences,
Korea Advanced Institute of Science and Technology, Daejeon, 305-701, Republic of Korea

[†]Department of Material Science and Technology,
Korea Advanced Institute of Science and Technology, Daejeon, 305-701, Republic of Korea
Email: siege0@nobelab.kaist.ac.kr

Abstract—Nonvolatile memory characteristics are presented with Ag nanocrystals (NCs) formed by a thermal decomposition process for a Flash memory application. A size of NC and a space of NC-to-NC were precisely controlled by a size-selective precipitation technique and the length of self-assembled monolayer surrounding NCs, respectively. The size and density of Ag NCs synthesized by the thermal decomposition were typically 3-5 nm and $2.7 \times 10^{12} \text{ cm}^{-2}$. Nonvolatile memory operations with relatively high speed and superior endurance characteristics were reported from NMOSFETs embedding metal NCs, which were fabricated by the gate last process.

Keywords – nonvolatile memory; flash device; thermal decomposition process and size-selective precipitation technique; metal nanocrystals

I. INTRODUCTION

A rapid growth of the market for mobile devices has required the high density and high performance nonvolatile memory (NVM) devices. In Flash memory, as the device shrinks below 45 nm, the nonvolatile characteristic was severely degraded due to the ultimately scaled gate dielectric thickness. Thus, it was proposed to use discrete storage nodes as a floating gate [1] and metal nanocrystals have received attention because of the high density of states and feasibility of work-function modulation of nanocrystals (NCs) by using various NC materials: silicon [1]-[3], germanium [4], [5], metal oxide [6], [7], and metal [8]-[10]. In this paper, uniformly well-ordered Ag NCs (workfunction=5.1 eV [11]) with high density ($2.7 \times 10^{12} \text{ cm}^{-2}$) were formed by the thermal decomposition process and size-selective precipitation technique [12]. The Ag NCs embedded NMOSFETs were fabricated by the gate last process, and fundamental memory characteristics were described.

II. DEVICE FABRICATION

Fig. 1 shows the process sequences and the dimensions for the Ag NCs embedded NMOSFET. After LOCOS isolation process, a mask oxide was patterned for Source/Drain (S/D) formation. Then, phosphorous S/D solid diffusion was performed and the mask oxide removed. Thereafter, a tunneling oxide was grown. Ag NCs by the thermal composition process and size-selective precipitation technique were spin-coated. For the synthesis of the Ag NCs, a mixture of a 5 mM of AgNO_3 , a 100 ml of oleylamine, and a 6 mM of oleic acid was refluxed at 130°C for 3 h. The size and density of the Ag NCs were controlled by the size-selective precipitation technique [12]. As shown in Fig. 2, after spin-coating of the prepared Ag NCs on the tunneling oxide, the transmission electron microscopy (TEM) was used for two different sizes and densities of Ag NCs—(a) 3-5 nm and $2.7 \times 10^{12} \text{ cm}^{-2}$, (b) 5-8 nm and $7.9 \times 10^{11} \text{ cm}^{-2}$. The crystal structure of the Ag NCs was identified by x-ray diffraction (XRD) analysis and, as shown in Fig. 2(c), the main peaks matched those of pure metallic face-centered-cubic (FCC) Ag. As a control gate dielectric, HfO_2 was deposited by plasma-enhanced atomic layer deposition (PEALD). And aluminum was deposited by RF magnetron sputter for a gate electrode and patterned.

III. RESULTS AND DISCUSSION

I_D - V_G characteristics of the Ag NCs embedded NMOSFET ($W/L=50/1.6 \text{ }\mu\text{m}$) were shown in Fig. 3. The gate voltage was double swept at the room temperature from negative to positive voltage and then from positive to negative voltage. The NCs embedded NMOSFET shows a large counterclockwise I-V hysteresis (ΔV_{th} is 7.5 V at +9/-9 V sweep), which clearly reveals the charge storage effect, as compared to 0.7 V for the control sample without Ag NCs. Fig. 4 shows the threshold voltage shift (ΔV_{th}) as a function of gate length (L_G) with fixed channel width ($W=50 \text{ }\mu\text{m}$) for the different double sweeping ranges from zero to 3, 5, 7, and 9 V. No device size dependency in ΔV_{th} reveals that uniformity of Ag NCs is satisfactory for a practical Flash memory application. In Fig. 5, the endurance characteristics were investigated. For an iterative Program/Erase (P/E), 80 μs pulses of (+9/-7 V) were repeatedly applied. Even with the relatively thick tunneling oxide ($t_{tunnel}=4.5 \text{ nm}$), a high P/E efficiency of 3 V window in V_{th} shift was achieved due to the high density of the Ag NCs. And a good endurance behavior was attained up to 10^7 cycles, even though electrons were accumulated after 10^6 cycles. Also, retention characteristics were shown in Fig. 6. 33% fraction of the stored charges in the Ag NCs was preserved at $5 \times 10^5 \text{ s}$. A poor retention time was mainly caused by leakage paths along the isolation boundary where the LOCOS oxide was recessed for the removal of S/D mask oxide. Retention characteristics can be improved by optimization of isolation process.

IV. CONCLUSION

Uniformly distributed Ag NCs of high density ($2.7 \times 10^{12} \text{ cm}^{-2}$) were achieved with the chemical synthesis and thermal decomposition method by utilizing size-selective precipitation technique. NMOSFETs embedding metal NCs were fabricated, and their nonvolatile characteristics were demonstrated. Despite of the relatively thick tunneling oxide ($t_{tunnel}=4.5 \text{ nm}$), 3 V of V_{th} window was obtained with 80 μs pulses of P/E voltage of +9/-7 V due to the high density of Ag NCs. Also, a superior endurance behavior of 10^7 cycles was accomplished.

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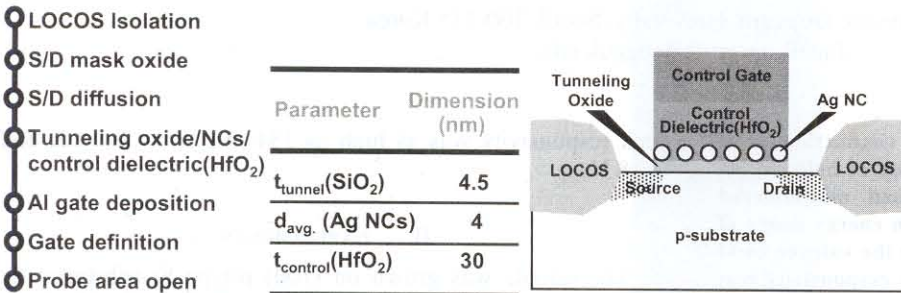


Fig. 1 Ag NCs embedded NVM process flow and dimensions used in this work and a Ag NCs embedded NMOSFET schematic

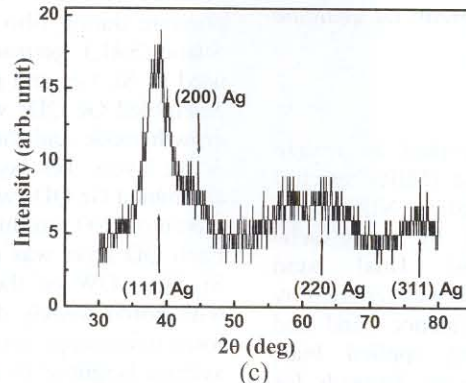
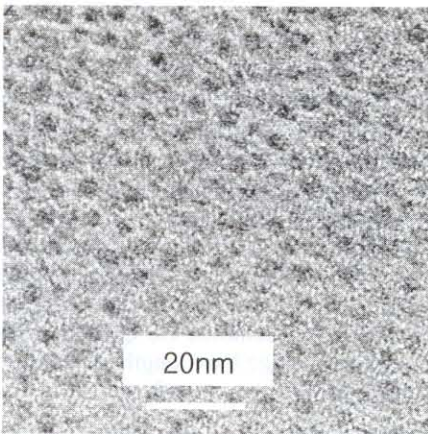


Fig. 2 TEM images of Ag nanocrystals which have the different size and density of (a) 3~5nm, $2.7 \times 10^{12} \text{cm}^{-2}$ and (b) 5~8nm, $7.9 \times 10^{11} \text{cm}^{-2}$. (c) XRD results of as-deposited Ag nanocrystals. It was identified that Ag nanocrystals were pure Ag from main peaks well matched with pure metallic FCC Ag peaks.

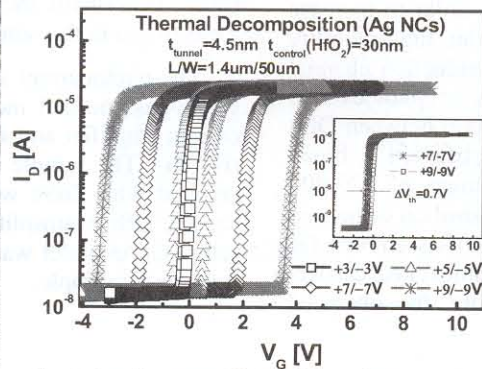
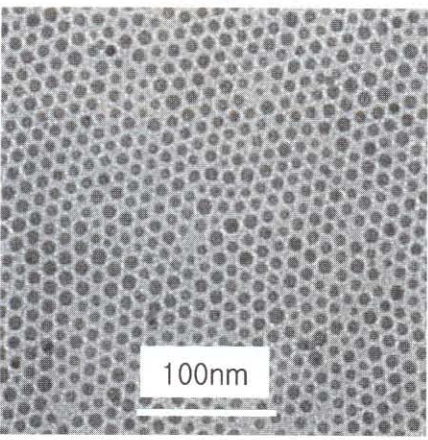


Fig. 3 Double swept V_G - I_D characteristic of $W/L=1.4/50 \mu\text{m}$ Ag NCs NMOSFET cell. The inset figure is showing V_G - I_D of NMOSFET without Ag NCs.

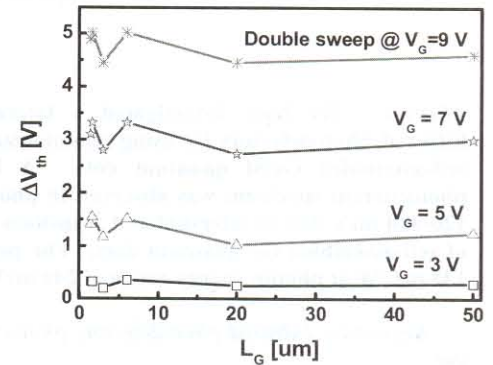


Fig. 4 V_{th} shift (ΔV_{th}) as a function of the gate length with the fixed width ($W=50 \mu\text{m}$) for the various sweeping ranges (from 0 to 3, 5, 7, and 9 V).

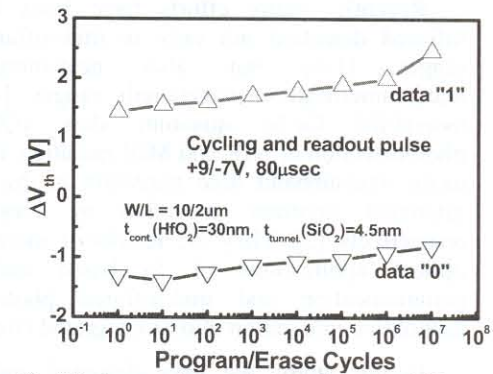


Fig. 5 Endurance characteristics with repeated 80 μs pulses of P/E voltage of +9/-7 V.

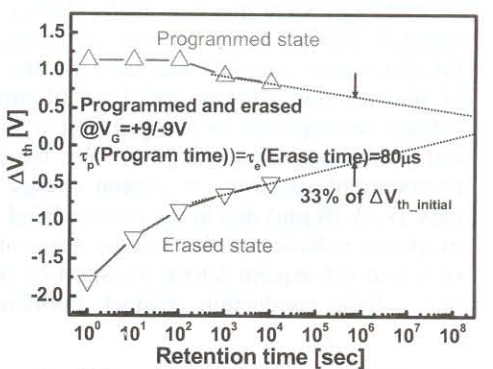


Fig. 6 Retention characteristics of the $W/L=10/2 \mu\text{m}$ Ag NCs NMOSFET cell at room temperature.