# Investigation of Gate Misalignment Effects in FinFETs

Kuk-Hwan Kim† , Jin-Woo Han and Yang-Kyu Choi‡

Dept. of EECS, Korea Advanced Institute of Science and Technology

373-1 Guseong-Dong Yuseong-Gu, Daejon, Korea

E-mail : † modestpe@nobelab.kaist.ac.kr ‡ ykchoi@ee.kaist.ac.kr‡

**Abstract** − Gate misalignment effects on electrical properties of FinFETs have been investigated with three-dimensional (3-D) mixed-mode simulator. A major trade-off between S/D series resistances and diffusion capacitances was induced by the gate misalignment. The influences of series resistances on short channel effects of few tens nanometer device are discussed in detail. A SOI FinFET and a body-tied FinFET were compared in terms of FO4 inverter delay to assess the gate misalignment effects on circuit performance as a whole. In the SOI FinFET, source series resistance is dominant factor in determining RC delay, while drain diffusion capacitance is more significant in the body-tied FinFET.

**Keyword** : Gate misalignment, FinFETs, Simulation, Mixed-Mode, Series resistence, Diffusion capacitance, FO4 delay

## *1. Introduction*

Double-Gate MOSFET (DGFET) has been considered as one of the most promising candidates for the channel length in the range of 10-30nm [1]. Even though planar double-gate transistors have higher scalability than their single gate counterparts because both gates help to control the potential in the body, gate misalignment between top and bottom gate may cause extra gate-to-S/D overlap capacitances as well as S/D series resistances [2]. In order to optimize the performance of double-gate devices, self-aligned processes and structures are proposed by using a single lithography and etch step, with FinFETs being one of the most pormising [3],[4]. However, FinFETs still suffer from congenital gate-to-S/D misalignment problem, in which gate pattern was not well aligned to delineated fin region.

It was found that this gate misalignment produces S/D asymmetric effects of series resistances and S/D-to-body diffusion capacitances. It is essential to understand the S/D asymmetric effects to optimize them in circuit design. In this paper, comprehensive analysis and optimization on the misalignment effects of FinFETs have been performed by using 3-dimensional device/mixed-mode circuit simulator with a calibrated carrier transport models in SILVACO® *Atlas*.

## *2. Series Resistance Analysis of Deep Sub-micron regime Device.*

A basic structure of FinFET in this simulation study is shown in **Fig.1**. In order to investigate effects of gate misalignment on device performance clearly, 100nm of extension length with no salicidation process is assumed. The critical geometrical parameters of the simulated FinFET are summarized in **Table 1**.

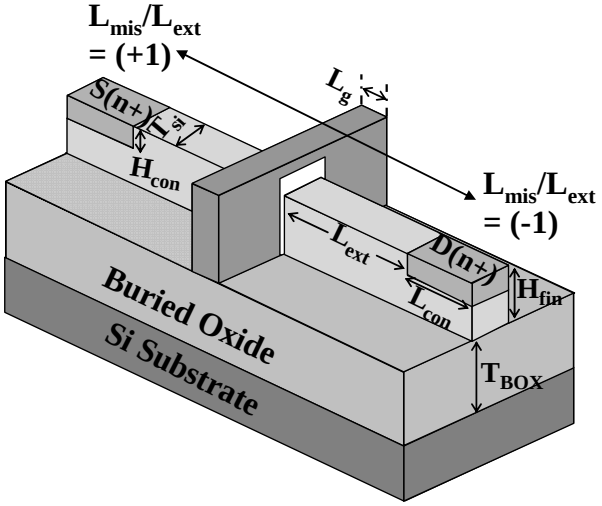


**Fig.1.** Simulated structure of SOI FinFET. $L_{mis}$ is defined as misalignment length compared to well aligned gate. "$L_{mis}/L_{ext}$ = (+1)" represents gate shift to source side completely, and "$L_{mis}/L_{ext}$ = (-1) to drain side. All the possible gate misalignment lies between above two extreme cases.

One of the major weaknesses in FinFETs is high series resistances caused by narrow and long fin topology. By incorporating effects of the S/D series resistances and carrier velocity saturation, a dain current ($I_D$) is simply expressed as follows:

$$I_{D,sat} = WC_{ox}v_{sat}(V_{GS} - V_T) = WC_{ox}v_{sat}(V_G - I_{D,sat}R_S - V_T)$$

$$I_{D,lin} = \frac{W\mu}{L}C_{ox}(V_G - V_T - \frac{1}{2}(V_D - I_{D,lin}(R_S + R_D))(V_D - I_{D,lin}(R_S + R_D))$$

**Table 1**. Parameters used for transistor simulations in this work.

- Gate Length ($L_g$) = 25nm
- Fin Thcikness ($T_{si}$) = 10nm
- Gate Oxide Thickness($T_{OX}$)=2nm
- Fin Height($H_{fin}$)=50nm
- Contact Length($L_{con}$)=70nm
- Contact Heignth ($H_{con}$) = 20nm
- Extension Length($L_{ext}$)=100nm for each side
- Buried Oxide Thickness($T_{BOX}$)=400nm
- Body Doping Concentration($N_{body}$)=5X10$^{15}$cm$^{-3}$
- Metal Gate Workfunction = 4.6eV

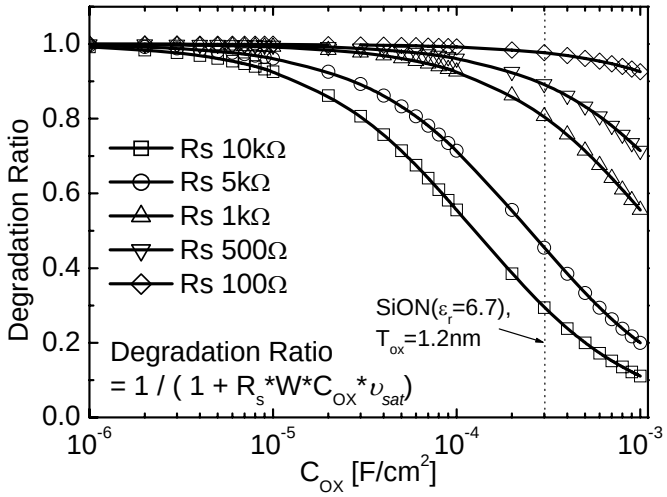


**Fig.2.** Degradation ratio defined as $I_{d,sat}$ without $R_{ext}$ over $I_{d,sat}$ with $R_{ext}$ versus $C_{OX}$.

Even though above two equations are hard to apply to few tens nanometer FinFETs, we can get intuition of series resistances effects on drain current with various $C_{OX}$. **Fig.2** plots a reduction ratio calculated by using above two equations versus $C_{OX}$ for various $R_S$. The reduction ratio is defined as ratio of $I_{D,sat}$ with $R_S$ to intrinsic $I_{D,sat}$ ($R_S$=0). As $C_{ox}$ becomes larger, a drive current is degraded more quickly by the S/D series resistances, and it implicates that as technology advances into a deep sub-micron regime, the S/D series resistances become major bottleneck in achieving the high drive current.

**Fig.3** shows the extension resistances as a function of the fin thickness with various S/D doping concentration by using the $R_{ext}$ extraction method proposed by *Jakub Kedzierski* et al. [5]. It was found that the extracted extension resistances increase sharply for below 20nm of fin thickness ($T_{si}$). **Fig.4** shows the extension resistances as a function of the fin thickness with gate misalignment. Error bar represents fluctuation of extension resistances by the gate misalignment. Note that as fin scales down, much fluctuation of extension resistances were induced by gate misalignment. It was worthwhile to note that

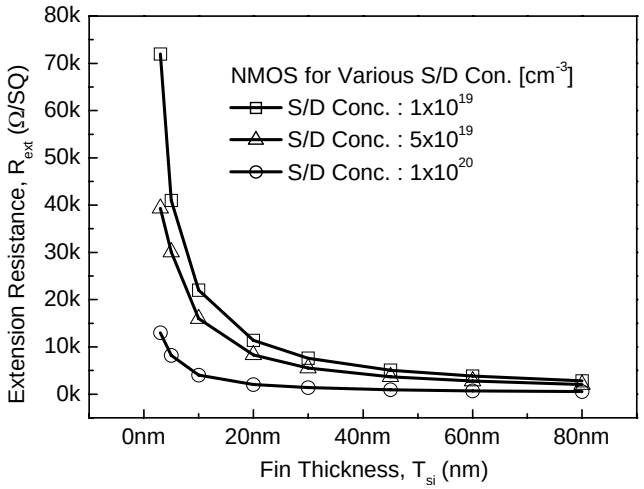


**Fig.3.** Extension resistance, $R_{ext}$ in Ohms/Square of extension, as a function doping concentration and fin thickness. A graphical demonstration of the $R_{ext}$ extraction method is presented in the reference [5].

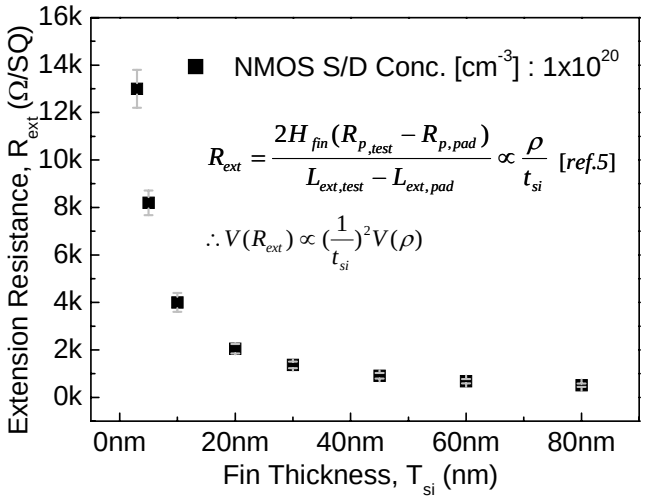


**Fig.4.** Extension resistance, $R_{ext}$ in Ohms/Square of extension, as a function gate misaslignment. Note that variation of ($R_S$+$R_D$) which is induced by gate misailgnment is within 10%, however, as fin scales down, fluctuation of extension resistances become severe.

the series resistances can cause performance degradation and reliability issues of few tens nanometer FinFET based on **Fig.3** and **Fig.4**,

### *3. Gate misalignment effects on saturation and linear region*

**Fig. 5** shows simulated the saturation current of FinFET and the drain current reduction as a function of gate misalignment with various gate oxide dielectrics. The drain current reduction is defined as ($1-I_{d,sat}/I_{d,sat(well\ algined)}$). For the case of the gate shift to the source side ($L_{mis}/L_{ext}$ = +1), the saturation current is maximized due to the reduced source extension resistance. The drain current reduction increases as the gate dielectric constant increases. This is because the potential drops by the S/D series resistance become larger as $I_{d,sat}$ ($g_{m,sat}$) increases. It was found that misaligned length

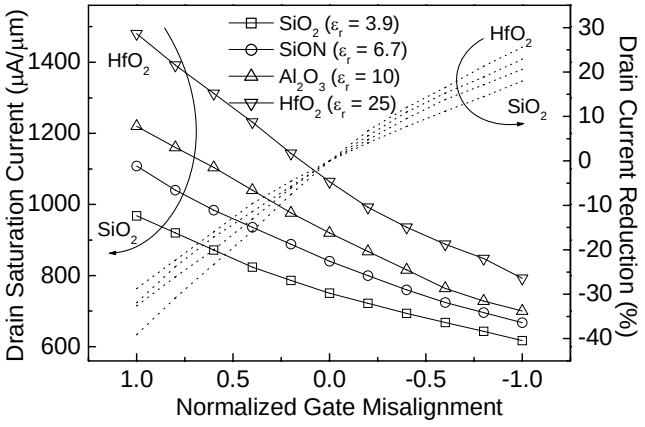


**Fig.5.** Satruation current versus normalized gate misalignment. The debiasing effect of $R_{ext}$ becomes stronger as $I_{D,sat}(g_{m,sat})$ increases.

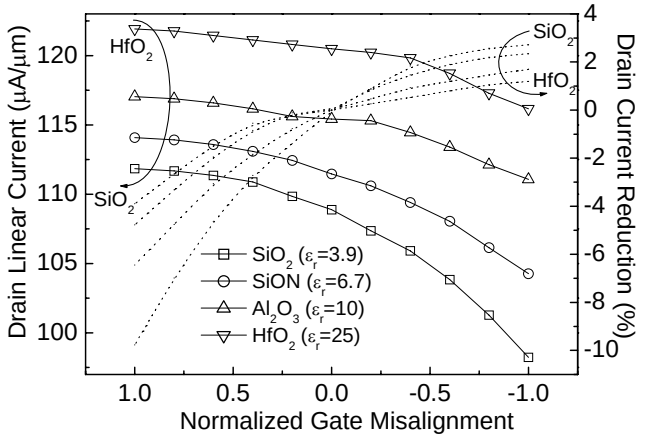


**Fig.6.** Linear current versus normalized gate misalignment.

($L_{mis}$) should be less than half of extension length ($L_{ext}$) in order to keep degradation of sautration current within 10%. **Fig. 6** plots the simulated linear current of FinFET and the drain current reduction as a function of the gate misalignment with various gate oxide dielectrics. In the linear region, the drain current was affected by both the effective $V_{GS}$ and $V_{DS}$. This explains why reduction of the drain current due to the S/D series resistance is significantly lower in the linear regime than in the saturation regime.

**Fig.7** shows the simulated nMOS $I_D$-$V_G$ characteristics of the FinFET. In comparison with the case of gate shift to drain side ($L_{mis}/L_{ext}$ = -1), the case of gate shift to source side ($L_{mis}/L_{ext}$ = +1) shows better short channel immunity. **Fig.8** shows an extracted DIBL and subthreshold slope at $V_{DS}$=0.05V and $V_{DS}$=1V as a function of normalized gate misalignment.The characteristics of DIBL and subthreshold slope at $V_{DS}$=1V are degraded as the gate is shifted from source side to drain side. **Fig.9** shows simulated potential at the channel center (depth=1/2*$T_{si}$) along a channel length direction

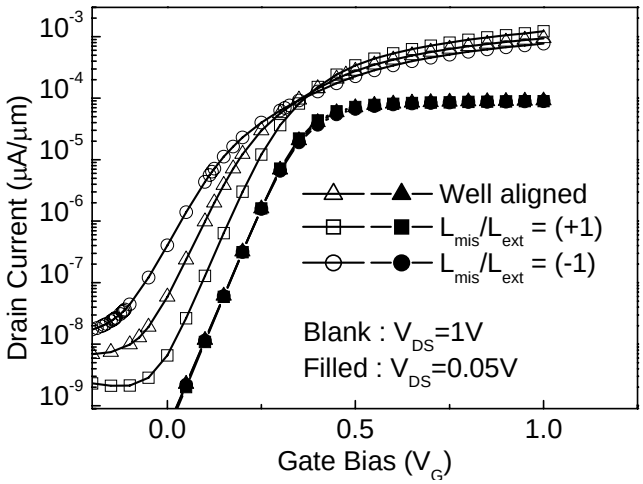


**Fig.7.** Simulated nMOS $I_D$-$V_G$ characteristics of FinFET. The $V_{DS}$ were 0.05V (filled symbol) and 1.0V (blank symbol), respectively.

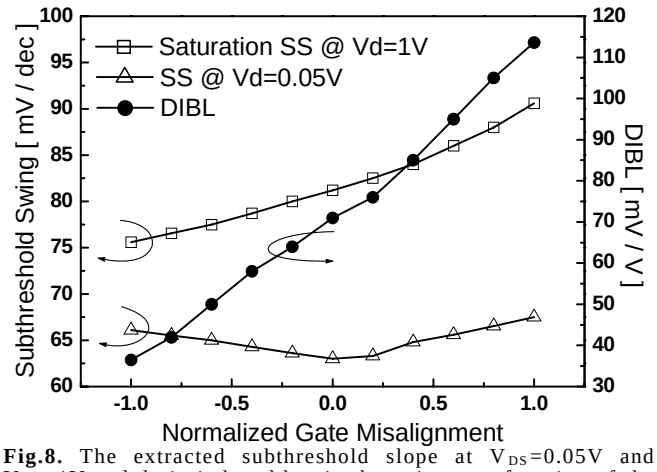


**Fig.8.** The extracted subthreshold slope at $V_{DS}$=0.05V and $V_{DS}$=1V and drain induced barrier lowering as a function of the normalized gate misalignment.

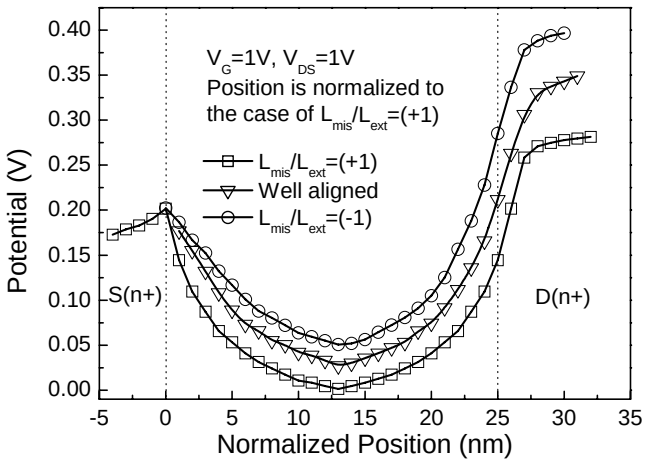


**Fig.9** The simulated potential at the channel center (depth=1/2*$T_{si}$) along channel length direction for $V_{GS}$ =1V and $V_{DS}$=1V.

for $V_{GS}$ =1V and $V_{DS}$=1V. It was found that as the gate shift from source side to drain side, a portion of the potential drop in the source resistance becomes bigger and an effective drain bias becomes larger. It results in

lowering the source-side carrier injection barrier and consequently increasing DIBL. Similarly, the subthreshold swing is degraded as the gate misalignment moves toward the drain side as well.

### *4. Circuit Performance in Body-Tied and SOI FinFET*

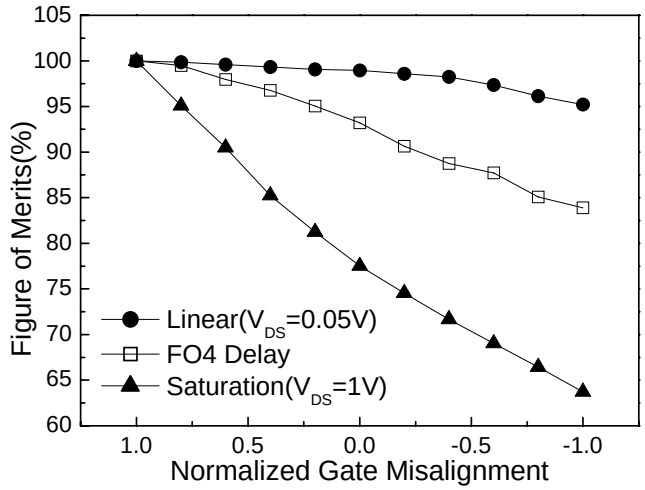


**Fig.10.** The extracted figure of merits of linear current, saturation current, and FO4 delay.

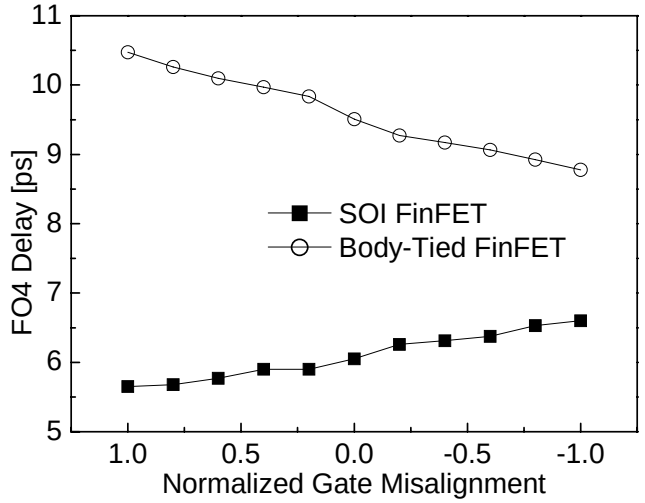


**Fig.11.** SOI FinFET and Body-tied FinFET are compared for FO4 delay versus normalized gate misalignment.

**Fig. 10** shows the extracted figure of merits of linear current, saturation current, and FO4 delay. Note that the speed figure of merit is closer to that of $I_{d,lin}$ rather it is to that of $I_{d,sat}$. This is because that devices in the ring oscillator do not spend as much time in the saturation region as in the linear region. **Fig.11** shows the SOI FinFET and the body-tied FinFET are compared for FO4 delay versus the normalized gate misalignment. The simulation results show that the body-tied FinFET presents worse FO4 delay rather than the SOI FinFET. And a trend of FO4 delay as a function of normalized gate misalignment is opposite. For the SOI FinFET, the effects of diffusion capacitance between drian to body are negligible. So, the condition for minimizing parasitic resistances is critical to reduce the RC delay in SOI FinFET. It was worthwhile to note that drain diffusion capacitance is more significant for RC delay in the body-tied FinFET. For the body-tied FinFET, a substrate was not floated but tied to the 0V. So, it was concluded that the coupling between S/D and substrate and, driven substrate can disturb the trasition of the drain node severely.

### *5. Conclusions*

In this paper, the gate misalignment effects on electrical properties of FinFETs have been investigated by using three-dimensional (3-D) mixed-mode simulator. Large S/D series resistances and sub-$V_T$ current of few tens nanometer can degrade the short channel effects such as subthreshold slope and DIBL. A major trade-off between S/D series resistances and diffusion capacitances was induced by the gate misalignment. In SOI FinFET, the source series resistance is a dominant factor in determining RC delay, while the drain diffusion capacitance is more significant in the body-tied FinFETs.

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