# 비대칭 이중 게이트를 이용한 한 셀당 2-비트를 저장하는 새로운 구조의 비휘발성 메모리

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**요약** 플래시 메모리 소자의 집적도를 두배로 증가시키기 위하여, 비대칭적인 일함수를 갖는 이중 게이트 구조 MOSFET과 금속-산화막-질화물-산화막-규소 (MONOS) 구조의 비 휘발성 메모리를 응용한 2-비트 동작을 하는 새로운 구조의 비휘발성 메모리 소자 구조 및 동작 조건을 제안, 최적화하였다. NAND 셀 배열 구조의 2-비트 프로그램 및 소거 동작은 독립적으로 제어되는 두개의 게이트를 이용한 Fowler-Nordheim (FN) 터널링을 이용하였다. 제안된 소자의 양쪽 게이트 일함수와 투과 산화막 두께의 변화를 통한 프로그램 상태의 문턱 전압 변화를 SILVACO® 시뮬레이션을 이용하여 연구하였다. 본 논문에서는 2-비트 동작을 위한 비대칭 이중 게이트 구조를 이용한 비 휘발성 메모리 소자에 대한 지침과 프로그램/읽기/소거 동작 조건을 제안하였다.

**키워드** : MONOS, Fowler-Nordheim tunneling, 비대칭 이중 게이트, 비 휘발성 메모리, 플래시 메모리

# Novel Structures for 2-Bit Per Cell of NVM Using Asymmetric Double Gate

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**Abstract** − A 2-bit operational metal-oxide-nitride-oxide-silicon (MONOS) nonvolatile memory using an asymmetric double-gate (ASDG) MOSFET is studied to double the flash memory density. The 2-bit programming and erasing is performed by Fowler-Nordheim (FN) tunneling in a NAND array architecture using individually controlled gates. A threshold voltage shift of programmed states for the 2-bit operation was investigated with the aid of SILVACO® simulator in the both sides of gate by changing gate workfunctions and tunneling oxide thicknesses. In this paper, guidelines of the 2-bit ASDG nonvolatile memory structure and operational conditions are proposed for “program”, “read”, and “erase”.

**Keyword** : MONOS, Fowler-Nordheim tunneling, Asymmetric double gate, Nonvolatile memory, Flash memory

## 1. Introduction

High density nonvolatile memory (NVM) is in tremendous demands of mobile and mass storage media market for low cost-per-bit needs. But, a scaling down of conventional NVM using floating gate structure is expected to face 45nm-barrier due to scaling limit of tunneling oxide thickness [1].

A silicon-oxide-nitride-oxide-silicon (SONOS) shows better scalability than a floating gate structure. But it will still suffer from the same scalability problems [2]. Multi-level cell or multi-bit cell nonvolatile memory is one of the promising structures to increase the density. It can circumvent the scaling problem. MONOS memory device has advantages of low programming voltage and better scalability. And the double gate MOSFET has been the most promising candidate for nano-scale regime due to a high robustness to short channel effects [3]. Individually controlled ASDG provides a simple multi-bit storage mechanism [4]. Four different gate bias conditions provide four programmed states “00”, “01”, “10”, and “11” by selectively charging the front and back gates of ASDG NVM.

In this paper, guidelines in adjusting the programmed threshold voltages are studied for various gate workfunctions and tunneling oxide thicknesses. And operational conditions of the ASDG NVM are verified and optimized with 2-D SILVACO® simulator for “program”, “read”, and “erase”.

## 2. ASDG gate NVM structure

Fig.1 shows cross-sections of ASDG NVM cell with different workfunctions of front gate (FG) and back gate (BG) materials with ONO (tunneling oxide/nitride /blocking oxide) structure. Tunneling oxide thickness is varied from 1nm to 4nm, and workfunction of FG is varied from 3.6eV to 4.6eV and that of BG is varied from 4.6eV to 6.2eV, which is higher than that of FG to distinguish bit1 and bit2. To program bit1, positive program bias is applied to FG and electrons are captured at tunneling oxide/nitride interface. And to program bit2, positive program bias is applied to BG. The threshold voltage shift from state “00”, i.e. no programmed state, is proportional to the amount of captured electrons in the nitride interface. The blocking oxide prevents the trapped electrons from leaking from the nitride to the gate. A nominal structure for the simulation has 100nm gate length ($L_G$), 10nm silicon film thickness ($T_{si}$), 4nm blocking oxide thickness, 5nm nitride thickness, and 1nm to 4nm tunneling oxide thickness.

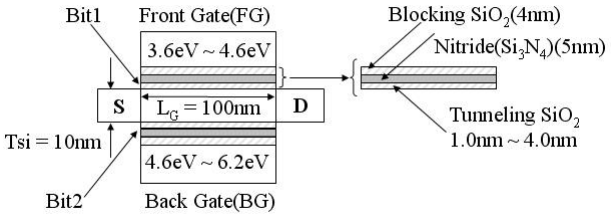


Fig.1. Schematics of ASDG NVM cell

## 3. Simulation results

In multi-bit memory, reading voltage is applied to the tied gates to find out the programmed state. Due to the different threshold voltages of each programmed state, distinguishable current values are measured correspondingly even though the same bias is applied to the tied gates. A wide window margin of programmed states is required to operate properly in the multi-bit cell. Fig.2 shows a reading current at different states with 4.1eV of the front gate workfunction ($WF_{FG}$) and 5.2eV of the back gate workfunction ($WF_{BG}$). It is more crucial to make a wide sensing window between “00” and “01” as

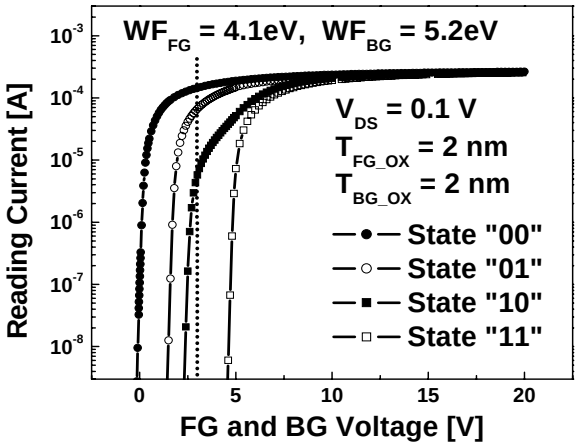


Fig.2. I-V characteristics of the ASDG cell programmed with the 4 distinguishable states of “00”, “01”, “10”, and “11”.

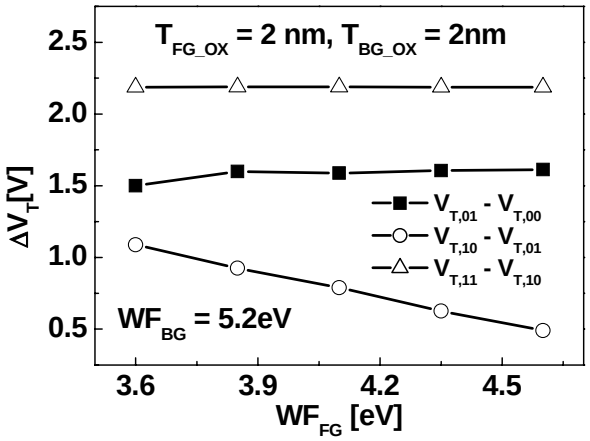


Fig.3. A shift of threshold voltage characteristics for various front gate workfunctions.

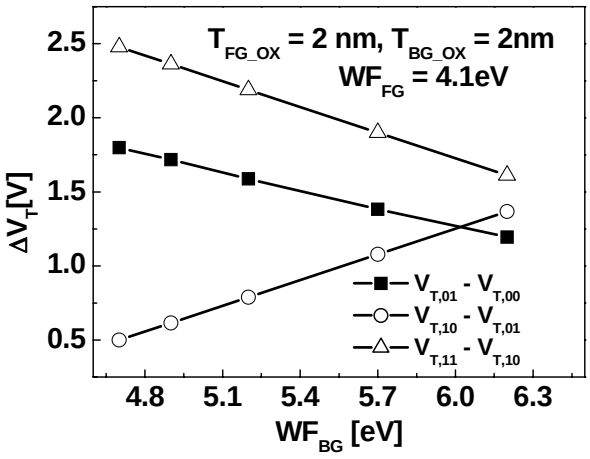


Fig.4. A shift of threshold voltage characteristics for various back gate workfunctions.

well as between “01” and “10” than between “10” and “11” in Fig.2.

Fowler-Nordheim (FN) tunneling is used to program the memory cell. Threshold voltage shift in “program” operation is used as the current window for the optimized process. The threshold voltage ($V_T$) is defined as a gate voltage read at 100nA drain current with $V_{DS}$ =50mV. $V_{T,00}$,$V_{T,01}$,$V_{T,10}$ and $V_{T,11}$ represent threshold voltages of programmed state “00”, ”01”, “10” and “11”.

Fig.3 and Fig.4 show the threshold voltage shift among adjacent 4-types of programmed states for various gate workfunctions. Fig.3 shows that $V_{T,10}-V_{T,01}$ increases as the $WF_{FG}$ decreases with the fixed 5.2eV of $WF_{BG}$. As the $WF_{FG}$ reduces, more electrons are trapped in nitride interface of FG side due to the lower barrier. Because the electric field from the FG to the channel is disturbed by the trapped electrons in the nitride interface, $V_{T,10}$ is increased and so does $V_{T,10}-V_{T,01}$. Fig.4 shows that $V_{T,01}-V_{T,00}$ decreases, and $V_{T,10}-V_{T,01}$ increases as the $WF_{BG}$ increases with the fixed 4.1eV of $WF_{FG}$. Similarly, these happen because the trapped electrons in nitride interface reduce due to the higher barrier height as the $WF_{FG}$ increases. Trade-off exists between $V_{T,10}-V_{T,01}$ and $V_{T,01}-V_{T,00}$ because of decreased $V_{T,01}$. From Fig.3 and Fig.4, small $WF_{FG}$ or moderate $WF_{BG}$ is preferable for the threshold voltage optimization.

Fig.5 and Fig.6 show the threshold voltage shift of neighboring programmed states for various tunneling oxide thicknesses with fixed 4.1eV of $WF_{FG}$ and 5.2eV of $WF_{BG}$. Fig.5 shows that $V_{T,10}-V_{T,01}$ increases as the thickness of FG tunneling oxide ($T_{FG\_OX}$) decreases. Because thinner $T_{FG\_OX}$ makes it easier to tunnel through the tunneling oxide, and more charges are trapped in the nitride interface. Fig.6 shows that $V_{T,01}-V_{T,00}$ decreases and $V_{T,10}-V_{T,01}$ increases as the thickness of BG tunneling oxide ($T_{BG\_OX}$) increases. With the decrement of $V_{T,01}$, $V_{T,01}$ approaches to $V_{T,10}$ but becomes more distant from $V_{T,00}$. In terms of the threshold voltage shift, 1nm of $T_{FG\_OX}$ and 4nm of $T_{BG\_OX}$ are the optimized tunneling oxide thicknesses. Also it is found that lowering workfunction results in the same effect with thinning the gate oxide thickness and vice versa.

Fig.7 shows the transient behaviors of threshold voltage of ASDG NVM cell during programming in four different states. A programming bias is selected to perform during the 10μsec($10^{-5}$sec). With $T_{FG\_OX}$=1nm and $T_{BG\_OX}$=4nm, programming bias of 15V is used to get 10 μsec programming time.

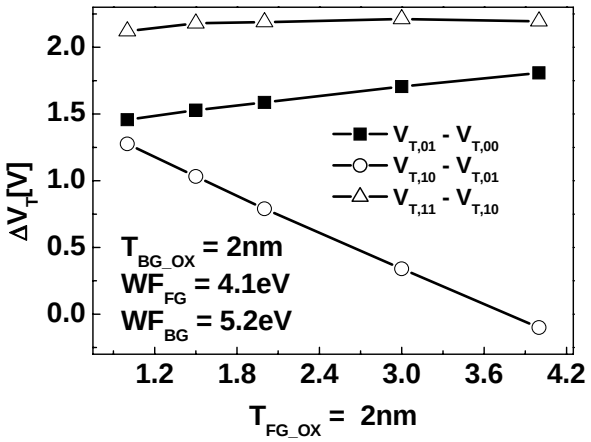


Fig.5. The shift of threshold voltage characteristics for various back gate oxide thickness.

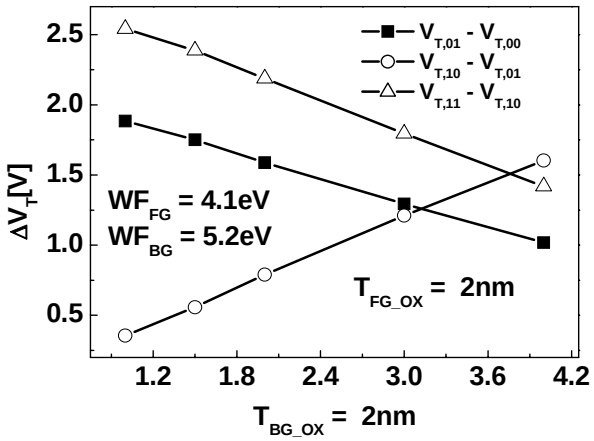


Fig.6. The shift of threshold voltage characteristics for various front gate oxide thickness.

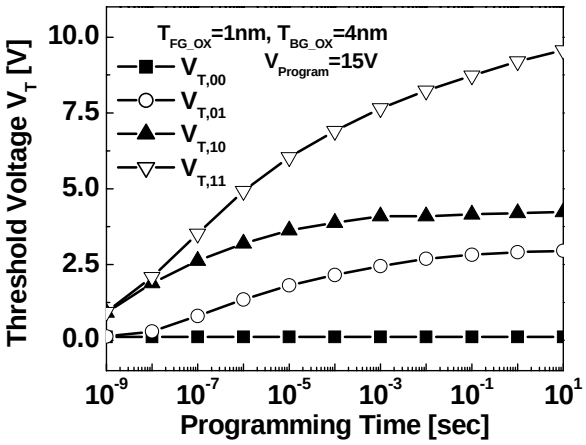


Fig.7. Transient behaviors of the $V_T$ during erase operation.

Table.1. The threshold voltage difference of neighboring states with programming time of 10μsec.

| Oxide Thickness [nm] | $V_{T,01}-V_{T,00}$ [V] | $V_{T,10}-V_{T,01}$ [V] | $V_{T,11}-V_{T,10}$ [V] |
|---|---|---|---|
| $T_{FG,OX}$= 1<br>$T_{BG,OX}$= 4 | 2.04 | 1.72 | 3.03 |
| $T_{FG,OX}$= 2<br>$T_{BG,OX}$= 2 | 2.44 | 0.98 | 3.59 |
| $T_{FG,OX}$= 1<br>$T_{BG,OX}$= 2 | 2.82 | 0.35 | 4.46 |

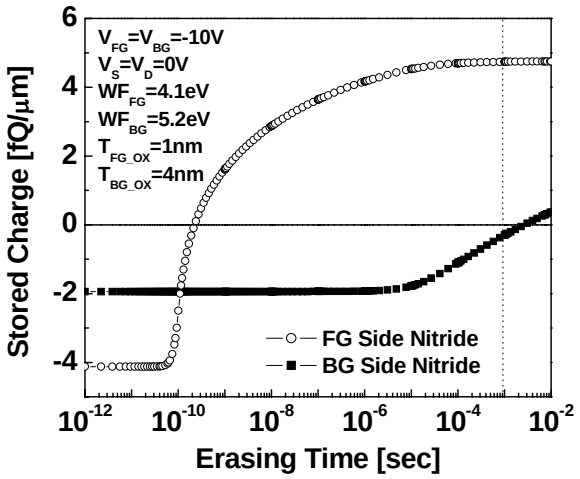


Fig.8. Transient behaviors of the stored charges at the interfacial nitride of FG and BG side during erase operation.

Table.2. The optimized bias condition that gives the 10 μsec programming time and 1msec erase time.

| operation | $V_{FG}$[V] | $V_{BG}$[V] | $V_{DS}$[V] |
|---|---|---|---|
| read | 2.7 | 2.7 | 0.1 |
| program "01" | 0 | 15 | 0 |
| program "10" | 15 | 0 | 0 |
| program "11" | 15 | 15 | 0 |
| erase | –10 | –10 | 0 |

Bit1 is more rapidly erased than bit2 due to the lower workfunction and thinner tunneling oxide thickness of FG side. Table 1 shows the threshold voltage difference of neighboring programmed states for various FG and BG tunneling oxide thicknesses with 10μsec programming time. To distinguish state “01” and “10”, the case of $T_{FG\_OX}$=1nm and $T_{BG\_OX}$=4nm shows the largest threshold voltage difference.

Negative gate with grounded channel erase (NGCE) method by FN-tunneling is used as an “erase” mechanism [5]. Fig.8 shows the transient behaviors of stored charges at FG and BG side nitride interfaces during “erase” operation. The optimized structure from programming condition is used. Two-bits are erased simultaneously from state “11” to state “00” with –10V of FG and BG bias and grounded source/drain. The figure shows the erasing speed of FG is faster than that of BG due to the lower workfunction and thinner tunneling oxide thickness. Due to the fast erasing, FG shows the characteristics of over-erase. But with NAND array cell, the over-erase is not in a big concern. To erase the stored data in ASDG NVM within 1msec, the “erase” voltage is –10V.

## 4. Conclusions

In this paper, ASDG NVM is proposed and optimized with various device parameters and read/program/erase operation conditions. To widen the current windows, asymmetric double gate with asymmetric tunneling oxide thickness is proposed. Finally, 4.1eV of $WF_{FG}$, 5.2eV of $WF_{BG}$, 1nm of $T_{FG\_OX}$, and 4nm of $T_{BG\_OX}$ are adopted as the optimized device parameters. The specific bias and time conditions of read/program/erase operation to perform the programming operation within the 10μsec and the erasing operation within the 1msec are shown in table.2. The ASDG NVM can become one of the major candidates of future non-volatile memory with the characteristics of 2-bit operation using conventional process.

## References


[1] L.Stefan, “Future Trends of Nonvolatile Memory Technology”, Intel press release, December 2001.

[2] C.C.Yeh, W.J.Tsai, T.C.Lu, Y.Y.Liao, N.K.Zou, H.Y.Chen, T.Wang, W.Ting, J.Ku, and C.Lu, “Reliability and Device scaling challenges of trapping charge flash memories”, Proceedings of 11th IPFA, 2004.”

[3] M.Ieong, H.Wong, E.Nowak, J.Kedzierski, E.C. Jones, “High Performance Double-Gate Device Technology”, Proc of ISQED, 2002.

[4] K.Yuen, T.Man, C.K.Alain, M.Chan, “A 2-Bit MONOS NonVolatile Memory Cell Based on Asymmetric Double Gate MOSFET”, IEEE EDL, vol.24, no.8, pp.518-520, August 2003.

[5] N.Kodama, K.Saitoh, H.Shirai, T.Okazawa, and Y. Hokari, "A 5Vonly 16Mbit Hash EEPROM cell using highly reliable write/erase technology", Symposium on VLSI Technology Dig.Tech.Papers, p.75, 1991.