Negative Bias Temperature Instability in SOI and Body-Tied Double-Gate FinFETs

Hyunjin Lee, Choong-Ho Lee, Donggun Park* and Yang-Kyu Choi*
Dept. of EECS, Korea Advanced Institute of Science and Technology, Daejeon 305-701, Korea
*Device Research Team, Semiconductor R&D Division, Samsung Electronics Co., Kyunggi-Do 449-711, Korea
Email:jinlee@eeinfo.kaist.ac.kr, Phone: +82-42-869-5477, Fax: +82-0505-869-3477

Abstract

Negative bias temperature instability (NBTI) characteristics of SOI and body-tied FinFETs are reported for the first time. Both FinFETs show better immunity to NBT stress at a wide fin width (channel thickness) than at a narrow fin width, while the narrow fin FinFET is more robust to hot-carrier injection (HCI) stress. A body-tied FinFET is more stable in response to NBT stress than a SOI FinFET because of non-floating body effects. CMOS lifetime is more degraded by NBT stress than by HCI stress at a narrow fin width and a low operational voltage.

Introduction

Double-gate structures showed high robustness to short-channel effects in the nano-scale regime [1-2]. Previous study showed that the reliability characteristics of CMOS SOI FinFETs by hot-carrier injection (HCI) stress improved with narrow fin width because of reduced impact ionization [3]. A recent report pointed out that NBTI became a major reliability concern for digital as well as analog CMOS circuits [4]. It is timely to study NBTI of double-gate or multiple-gate structures. This work primarily focused on the reliability under NBT stress for double-gate structures: SOI FinFETs and body-tied FinFETs. The fin width is a crucial parameter for determining the device degradation by NBT stress, and a wide fin is preferred to improve the reliability. A simple explanation for device degradation by NBT stress is presented and a specific limiting factor (NBTI or HCI) to govern the device failure is analyzed.

Experiments

The schematic device structures of the SOI and body-tied FinFET under NBT stress conditions are shown in Fig. 1. Negative bias was applied to the gate with grounded source/drain for SOI and body-tied FinFETs. Additionally, the body (substrate) was grounded and maintained at 125°C (high temperature test) for the body-tied FinFETs. Fabrication details were already reported elsewhere [1-2]. The NBTI characteristics had been interpreted using electrochemical reaction models at the SiO_2/Si interface [5-6]. Hydrogen-passivated dangling silicon bonds are electrically activated by holes at the interface. Then, active interface traps and positive fixed oxide charges are left, while electrons diffuse toward the center of the fin in the SOI FinFETs or the substrate in the body-tied FinFETs. A threshold voltage (V_T) was read at -100nA drain current with -50mV drain bias. V_{TO} is the threshold voltage before NBT stress. The criterion for failure lifetime is 10% degradation of the drain saturation current (I_{Dsat}), i.e. $\Delta I_{Dsat}/I_{Dsat0}$=10%. I_{Dsat0} is the drain saturation current before DC NBT stress.

Results and Discussions

The degradation of I_{Dsat} and V_T of the PMOS SOI FinFET is accelerated as the DC negative stress voltage is increased or the fin width of FinFET is narrowed (Fig. 2, 3). When the negative gate bias is applied, the electrons generated by this stress are pushed back to the center of the silicon fin and accumulate as shown in Fig. 4. As the fin width decreases, the energy band bending due to the accumulated electrons at the center of the silicon fin becomes steeper [7]. The sharp energy band bending increases hole concentration at the interface, and results in accelerating NBTI. This trend is consistent with the previous expectation [8]. Since immunity to NBT stress improves with wider fin width, it should be optimized in balance with short-channel effects (SCEs), to which the wider fin is vulnerable. Fig. 5 and 6 show the device lifetime of the SOI and the body-tied FinFETs with different fin widths. The lifetime of the both FinFETs is more seriously degraded for the narrow fin, and the lifetime slope of the body-tied FinFET is steeper (longer lifetime) than that of the SOI FinFET due to the grounded substrate. In cases of the grounded body-tied FinFETs, the electrons move toward the ground substrate rather than the center of the silicon fin, and there is no extra band bending to increase hole concentration at the interface. To verify this simple model, -0.2V was applied to the substrate of the body-tied FinFET. In this bias condition, the electrons are likely floating, thus the lifetime was degraded in the same manner as the SOI FinFETs. Fig. 7 and 8 show the temperature dependency of the NBTI at the SOI FinFETs. The device degradation by NBT stress is thermally exacerbated [6]. The device immunity against NBT stress can be improved by adopting a wide fin width and a low operational temperature. In comparison to 0.1μm-technology single-gate bulk-FET [7] with the 39nm SOI FinFET as well as the 30nm body-tied FinFET, the SOI FinFET shows worse NBTI than both the single-gate bulk-FET and the body-tied FinFET due to the existence of floating electrons as shown in Fig. 9 and Fig. 10. Behaviors of the generated electrons due to the NBT stress rule the device lifetime degradation rate. Unlike SOI FinFET, the body-tied FinFET is not readily damaged by NBT stress even at a high operational temperature. Fig. 11 shows that the NBTI is important in p-channel FinFETs at low V_{DD} and HCI is concerned in n-channel FinFETs at high V_{DD} [3][9]. Critical voltage, a cross point of the two degradation mechanisms, NBTI and HCI, increases incrementally with operational temperature. And the critical voltage range of W_{Fin}=30nm ($V_{CR,30}$ range) is larger than that of W_{Fin}=34nm ($V_{CR,34}$ range) in Fig. 12. These results represent that high substrate temperature or narrow fin FinFET induces NBTI as a limiting factor of device failure rather than HCI. The critical voltages are plotted as a function of the gate oxide thickness and fin width in Fig. 13. At the wide fin width (W_{Fin}=34nm), the supply voltage according to the ITRS roadmap is larger than the critical voltage. Therefore, HCI limits the device lifetime in both FinFETs. However, when the fin width is reduced (W_{Fin}=30nm), the lifetime degradation by NBT stress becomes dominant.

Conclusions

Device lifetime degradation by NBT stress was investigated on SOI and body-tied FinFETs for the first time. The degradation is more significant for the narrow fin than the wide fin. The body-tied FinFET shows better immunity against the NBT stress due to non-floating body effects. As the fin width is narrowed for further device scaling, NBTI starts to limit the device lifetime in the PMOS FinFETs while the lifetime degradation by HCI improves.

Acknowledgment

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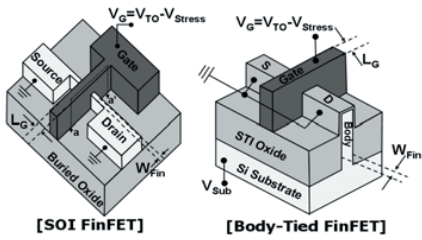

Fig. 1. Schematic device structures of the SOI FinFET and the body-tied FinFET under NBT stress conditions.

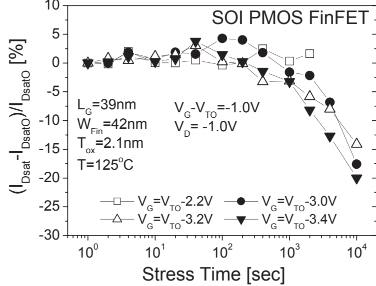

Fig. 2. I_{Dsat} degradations vs. stress time for different DC negative stress voltages in the PMOS SOI FinFET. (L_G=39nm, W_{Fin}=42nm).

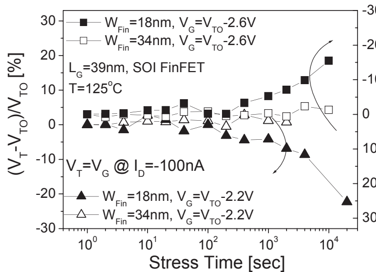

Fig. 3. V_T degradations vs. stress time for different stress voltages and fin widths. Narrow fin FinFET shows worse immunity to NBT stress.

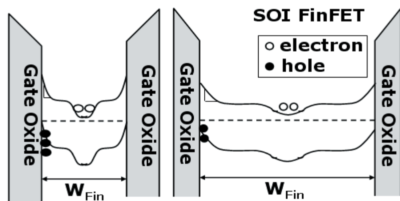

Fig. 4. Schematics of energy band diagram of the narrow fin and wide fin SOI FinFETs along a-a' direction in Fig.1. A steeper band bending is shown at the narrow fin.

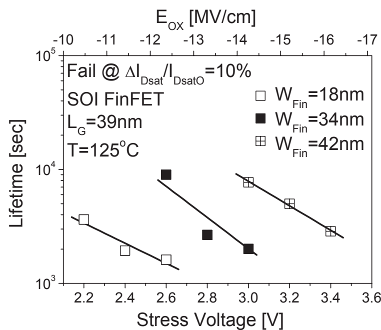

Fig. 5. DC lifetime by NBTI vs. stress voltage for the SOI FinFETs (L_G=39nm and W_{Fin}=18nm, 34nm, and 42nm). The wider fin FinFET shows longer lifetime.

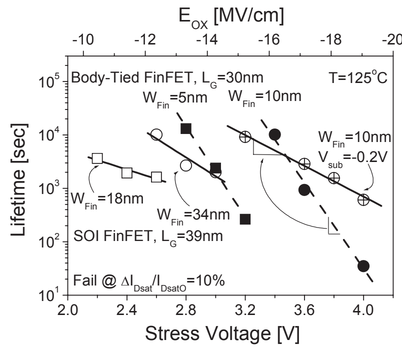

Fig. 6. DC lifetime by NBTI vs. stress voltage for the SOI and the body-tied FinFETs with different fin widths. Cross marked circles represent the body-tied FinFETs with V_{sub}=-0.2V. The slope is lowered by the negative substrate bias.

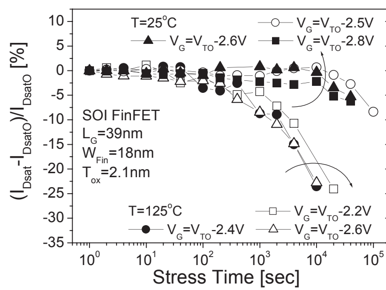

Fig. 7. I_{Dsat} degradations vs. stress time for the different stress bias and the substrate temperatures (W_{Fin}=18nm). The degradation is more at a high operational temperature.

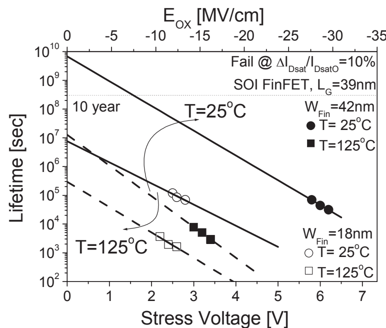

Fig. 8. DC lifetime by NBTI vs. stress voltage and E_{OX} in the SOI FinFETs (W_{Fin}=18nm, 42nm, and the substrate temperatures=25°C, 125°C, respectively).

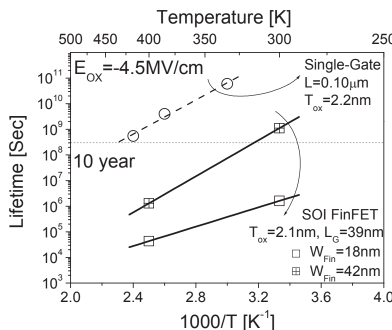

Fig. 9. Comparison of DC lifetime by NBTI between the single-gate bulk-FET [7] and the SOI FinFETs with a function of substrate temperature.

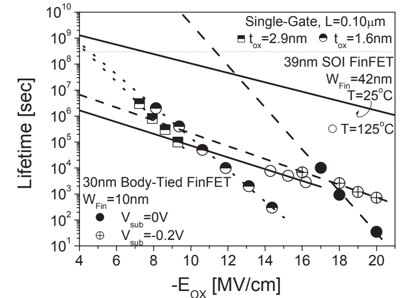

Fig. 10. DC lifetime by NBTI of single-gate bulk-FET [7], SOI FinFET, and body-tied FinFET. Symbols represent the lifetime at 125°C, and solid line without symbols represents the SOI FinFET lifetime at 25°C.

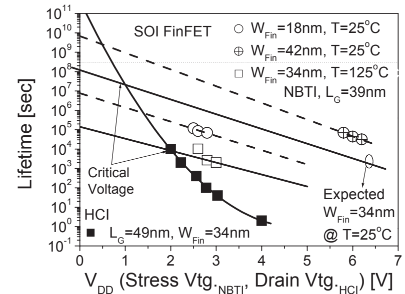

Fig. 11. DC lifetime is governed by two degradation mechanisms: HCI [1] and NBTI at 25°C and 125°C, as a function of supply voltage, V_{DD} .

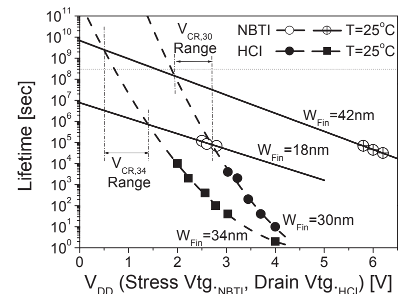

Fig. 12. A Critical voltage, a cross point of HCI [1] and NBT with different fin widths to identify a limiting factor to govern the lifetime in the SOI FinFETs (W_{Fin}=30nm and 34nm).

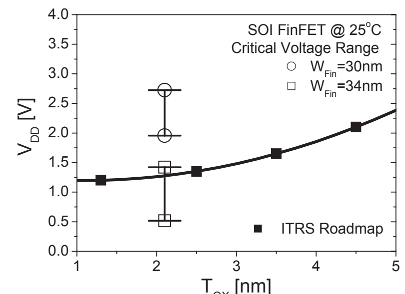

Fig. 13. Transition of a limiting factor to govern the lifetime of CMOS FinFETs. As the fin width decreases, the limiting factor changes from HCI to NBTI.