Multiple-Gate MOSFETs 의 Punchthrough 특성에 대한 포괄적 연구

- SOI MOSFET 의 여러가지 게이트 형태에 따른 punchthrough 전압의 경향성 -

강현식, 류승완, 최양규

한국과학기술원 전자전산학과, 대전광역시 유성구 구성동 373-1

E-mail: ooohihi@nobelab.kaist.ac.kr

요약 서로 다른 게이트 구조를 가지는 SOI FinFET 의 punchthrough 특성에 관하여 연구하였다. FinFET 의 단채널특성을 결정짓는 fin 폭의 변화에 대한 punchthrough 전압을 측정하였고, 그 측정치를 3-D Silvaco 시뮬레이션 결과와 비교하였다. 시뮬레이션을 통해 다양한 게이트 구조의 SOI FinFET (전형적인 FinFET, Π-게이트 FinFET, Ω-게이트 FinFET, all-around-게이트 FinFET) 에 대한 punchthrough 전압을 비교하였다. 게이트가 채널 전면을 감싸고 있는 all-around-게이트 구조의 경우, 누설 경로가 줄어들게 되어 결과적으로 punchthrough 에 강한 소자 특성을 보이게 된다. 소자 스케일링에 따른 누설전류 영향을 줄이고 punchthrough 특성을 개선하기 위해서는 all-around-게이트 SOI FinFET 의 구현이 필요하다.

키워드 Punchthrough, SOI, FinFET, Multiple-gate, Fin 폭

A Comprehensive Study of Punchthrough Characteristics in Multiple-Gate MOSFETs

- The Trend of Punchthrough Voltages in Various Gate Shapes of SOI MOSFETs -

Hyun-Sik Kang, Seong-Wan Ryu and Yang-Kyu Choi

Dept. of EECS, KAIST 373-1 Guseong-Dong, Yuseong-Gu, Daejeon, Korea

E-mail: ooohihi@nobelab.kaist.ac.kr

Abstract Punchthrough characteristics are investigated for different gate structures on silicon-on-insulator (SOI) FinFET. The punchthrough voltage (V_{PT}) was measured and verified by 3-D Silvaco simulator for various fin widths, crucial parameter to govern short-channel effects. The simulated results show a good agreement to the experimental data. Thereafter, the punchthrough voltages for multiple-gate structures in the SOI FinFETs: conventional FinFET, Π-gate FinFET, Ω-gate FinFET and all-around-gate FinFET, were simulated with the aid of the Silvaco simulator after verification with experimental data. When the overlapped area of the gate-channel straddling the body increases, leakage paths reduce, and the punchthrough voltages increase as a result. For aggressive device scaling, all-around gate is highly preferable.

Keyword Punchthrough, SOI, FinFET, Multiple-gate, Fin Width

1. Introduction

As the MOSFET scales down into the nano scale regime, short-channel effects (SCE) and poor subthreshold characteristics begin to retard evolution of traditional planar transistors [1]. When the channel length decreases aggressively, the off-state leakage current rapidly increases by drain induced barrier lowering (DIBL). Subthreshold current has an exponential dependence on the potential barrier, so that even small reduction of barrier substantially degrade the turn-off characteristics [2]. Thus, the multiple-gate structures are highly attractive because of the suppression of the SCE [3]. Even though both of DIBL and subthreshold leakage are important parameters for deep-sub-tenth micron devices, punchthrough characteristics have not been

investigated yet. In this paper, the punchthrough characteristics of a SOI FinFET are studied intensively. Because of a steep subthreshold slope and excellent suppression of SCE, a fully-depleted SOI FinFET has received attention for sub-100nm CMOS applications [4]. And, a FinFET was well known to reduce the leakage current effectively because of elimination of leakage paths due to the double-gate. The dependence of punchthrough voltages (V_{PT}) on various fin widths (W_{FIN}) was investigated. It was correlated by measured data, then verified by 3-D Silvaco simulator [5]. It was found that the channel potential is sensitive to the W_{FIN} [6]. Afterward, from a conventional SOI FinFET to an all-around-gate (A-G) SOI FinFET, the punchthrough characteristics are studied by the verified Silvaco simulator.

2. Device Design

In Fig.1, the SOI FinFETs have 88nm gate length (L_G), 2nm thickness of gate oxide and $1x10^{17}cm^{-3}$ concentration of body (N_{BODY}). Fig.1(a) shows a schematic and cross-sectional view of the conventional SOI FinFET. The fabrication details for the conventional FinFET of Fig.1(a) were previously reported elsewhere [7][8].

Fig.1(b) shows a Π-gate SOI FinFET [9]. The gate structure is similar to Π shape, due to the over-recess of the buried oxide (BOX). And, when the fin is patterned, it is usually over-etched isotropically by pre-cleaning before gate dielectric formation. Thus, the fin profile becomes Ω-shape as shown in Fig.1(c) [10]. In the all-around-gate SOI FinFET, gate wraps all around Si body, which is floating absolutely from the BOX as shown in Fig.1(d).

3. Results and Discussion

3.1 The punchthrough voltages in multiple-gate structures.

Fig.2 shows the punchthrough voltages (V_{PT}) of measured data, and it was matched with 3-D simulated values for various W_{FIN} (26nm, 34nm and 42nm) in both fabricated NMOS and PMOS SOI FinFETs. The V_{PT} which is a drain bias was read at 100nA of drain current for grounded source and gate. As the W_{FIN} reduces, the V_{PT} increases due to the increments of gate-to-channel potential controllability. The simulation data has a good agreement to the measured data. Now, 3-D simulation is correlated by the experimental data.

The cross-sectional views of the 4-types SOI FinFET along a-a' direction are shown in Fig.1. When the δW_{FIN} is made by the undercut profile, the gate structure starts to make the Ω-gate FinFET. And, when the δW_{FIN} meets together at the both sides, the all-around-gate FinFET is formed. The conventional FinFET, Π-gate FinFET, Ω-gate FinFET and all-around-gate FinFET are denoted by Type Ⅰ, Type Ⅱ, Type Ⅲ and Type Ⅳ in short, respectively. And Fig.3(a) shows the punchthrough voltages at different gate structures for various W_{FIN} (26nm, 34nm and 42nm) in NMOS SOI FinFETs. As channel area is increasingly surrounded by the gate, the leakage paths are reduced, due to a pinching effect of an electric field from drain through the BOX. Thus, as the gate structure evolves from Type I to Type IV, the V_{PT} rapidly increases for various W_{FIN}. It is found that the narrow W_{FIN} is more effectively influenced by the gate structure of all types. In Fig.3, for more intensive study, the V_{PT} dependence on the δW_{FIN} is simulated in detail for the Ω-gate FinFET. As the δW_{FIN} increases, the V_{PT} increases linearly. In Fig.4, the V_{PT} dependence on body doping concentration (N_{BODY}) for the all-around-gate FinFET is investigated additionally. The V_{PT} increases as the body doping concentration increases because electric field coming from the drain is pinched [11].

3.2 The short-channel effects (SCE) in multiple-gate structures.

Fig.5 shows DIBL and off-state leakage current (I_{OFF}) of the SOI FinFET for 4-types of structure. As the gate structure evolves to the all-around-gate FinFET, the DIBL is suppressed quickly, which represents good robustness to the threshold voltage fluctuation. Furthermore, in the off-state, the reduced leakage current results in rising of V_{PT}.

Fig.6 shows subthreshold slope (SS) of the SOI FinFET at V_D=1.0V and V_D=0.05V for 4-types of structure. As the gate structure evolves to the all-around-gate FinFET, the SS decreases. This decrement of the SS for the all-around-gate FinFET can be interpreted as a result of the increment of gate controllability [12].

These results show that the all-around-gate FinFET is effective in suppressing the SCE, and aggressive device

scaling.

4. Conclusion

The punchthrough voltage is found to be improved by reduction of the W_{FIN} after measurement and 3-D simulation. And, through 3-D simulation for various gate structures of SOI FinFET, we understand punchthrough behavior in the multiple-gate FinFET. Afterward we have also investigated DIBL, subthreshold slope in the multiple-gate FinFET. As the device structure evolves from the conventional FinFET to the all-around-gate FinFET, the higher V_{PT} is achieved, and DIBL and subthreshold slope are improved. Based on these results, we conclude that the all-around-gate SOI FinFET is the most promising for deep-sub-tenth micron era.

References

[1] C. P. Auth, J. D. Plummer, " Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFET's ", IEEE Electron Device Letters, vol. 18, pp. 74-76, 1997.

[2] G. Taylor, " Subthreshold conduction in MOSFET's. ", IEEE Trans. on Electron Devices, vol. 25, pp. 337-350, 1978.

[3] J.-P. Colinge, M.-H. Gao, A. Romano, H. Maes, C. Claeys, " Silicon-on-insulator gate-all-around device ", IEEE IEDM Tech. Dig., pp. 595-598, 1990.

[4] J.-T. Park, J.-P. Colinge, " Multiple-gate SOI MOSFETs: Device design guidelines ", IEEE Trans. on Electron Devices, vol. 49, pp. 2222-2229, 2002.

[5] Silvaco International, ATLAS User's Manual, 2002.

[6] H. Wang, M. Chan, Y. Wang, P. K. Ko, " The behavior of narrow-width SOI MOSFETs with MESA isolation ", IEEE Trans. on Electron Devices, vol. 47, pp. 593-600, 2000.

[7] Y.-K. Choi, N. Lindert, X. Peiqi, S. Tang, D. Ha, E. Anderson, T.-J. King, J. Bokor, C. Hu, " Sub-20 nm CMOS FinFET Technologies ", IEEE IEDM Tech. Dig., pp. 421-424, 2001.

[8] X. Wu, P. C. H. Chan, S. Zhang, C. Feng, M. Chan," Stacked 3-D fin-CMOS technology ", IEEE Electron Device Letters, vol. 26, pp. 416-418, 2005.

[9] J.-T. Park, J.-P. Colinge, C. H. Diaz, " Pi-gate SOI MOSFET ", IEEE Electron Device Letters, vol. 22, pp. 405-406, 2001.

[10] F.-L. Yang, H.-Y. Chen, F.-C. Chen, C.-C. Huang, C.-Y. Chang, H.-K. Chiu, C.-C. Lee, C.-C. Chen, H.-T. Huang, C.-J. Chen, H.-J. Tao, Y.-C. Yeo, M.-S. Liang, C. Hu, " 25nm CMOS omega FETs " IEEE IEDM Tech. Dig., pp. 255-258, 2002.

[11] B. Cheng, B. Maiti, S. Samavedam, J. Grant, B. Taylor, P. Tobin, J. Mogab, " Metal gates for advanced sub-80-nm SOI CMOS technology ", IEEE Int'l SOI Conf., pp. 91-92, 2001.

[12] R. Gwoziecki, T. Skotnickt, " Physics of the subthreshold slope-initial improvement and final degradation in short CMOS devices ", ESSDERC, pp. 639-642, 2002.

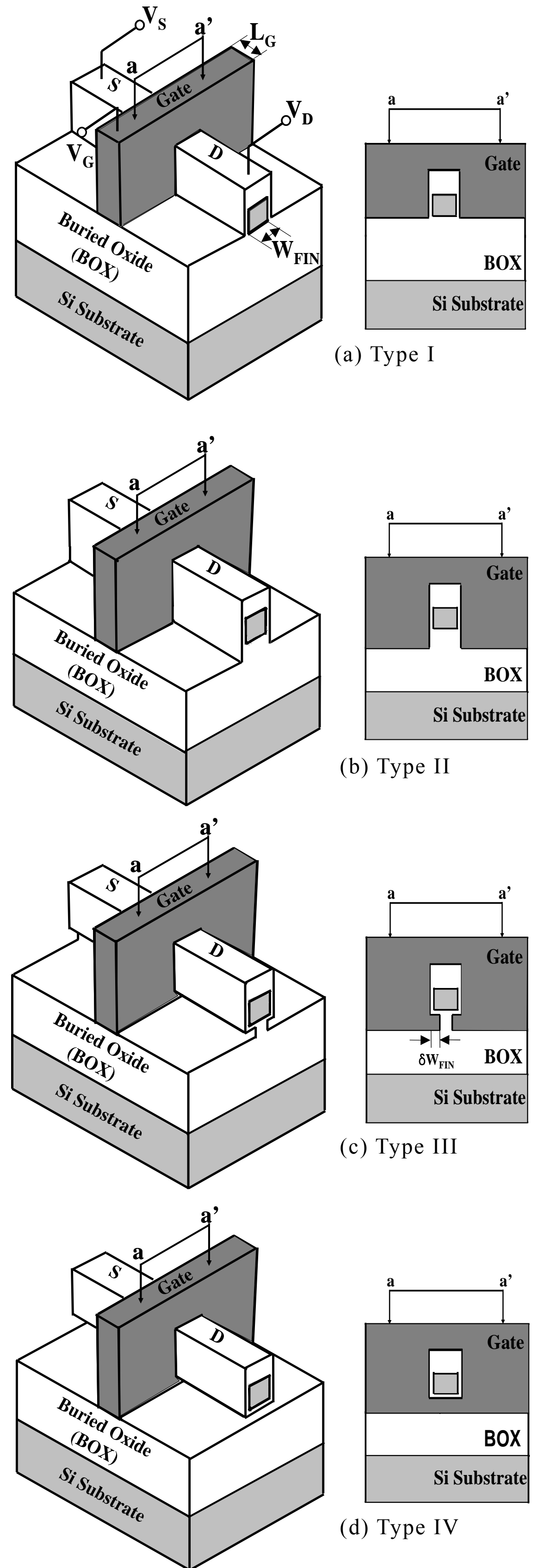


Fig.1 3-D schematics and the cross-sectional views along a-a' direction for the multiple-gate SOI FinFET structures. (a) the conventional FinFET. (b) the Π-gate FinFET. (c) the Ω-gate FinFET. (d) the all-around-gate FinFET.

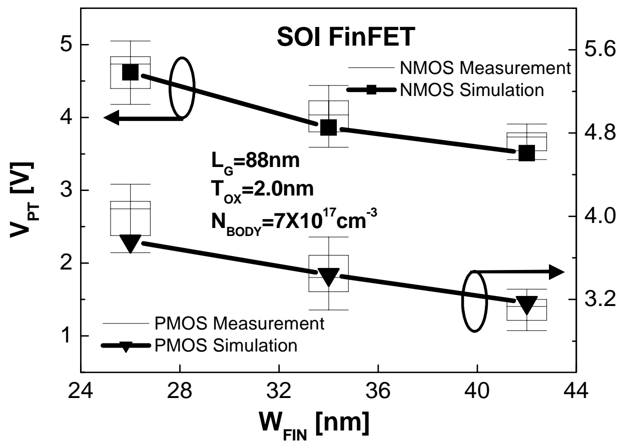


Fig.2 Dependence of the punchthrough voltages (V_{PT}) on various fin widths (26, 34, 42nm) in both NMOS and PMOS SOI FinFETs.

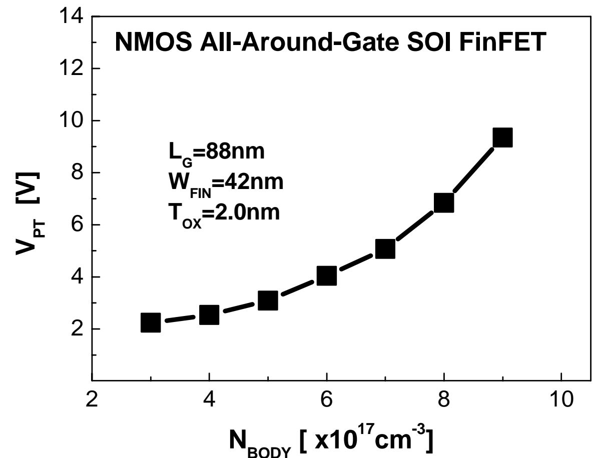
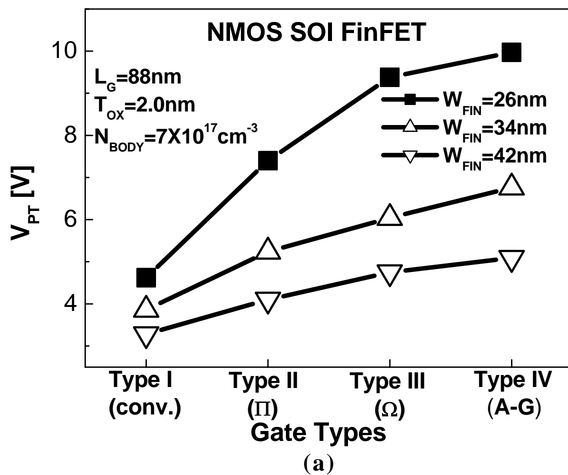
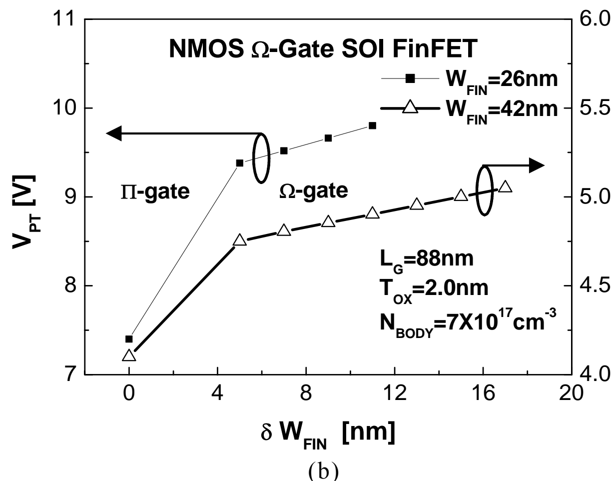


Fig.4 3-D simulated punchthrough voltages (V_{PT}) for different body doping concentration in the NMOS all-around-gate SOI FinFET. As the N_{BODY} increases, the V_{PT} increases.



(a)



(b)

Fig.3 3-D simulated punchthrough voltages (V_{PT}) for (a) 4-types of structure and (b) various δW_{FIN} of the Ω-gate SOI FinFET. From Type I to Type IV, better punchthrough immunity is obtained.

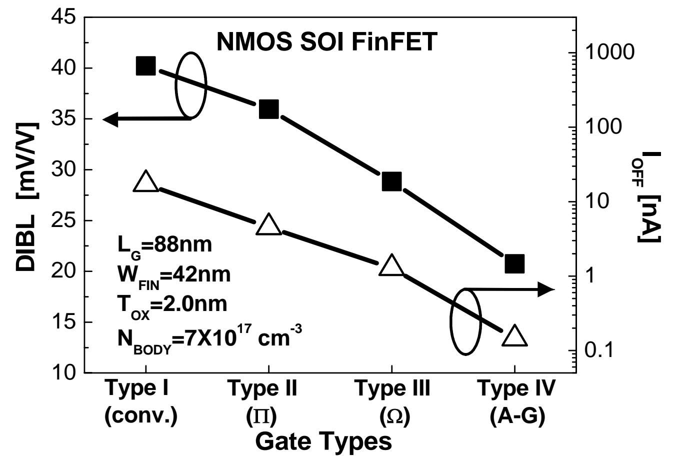


Fig.5 3-D simulated DIBL and off-state leakage current (I_{OFF}) for 4-types of structure. From Type I to Type IV, better DIBL effect is obtained.

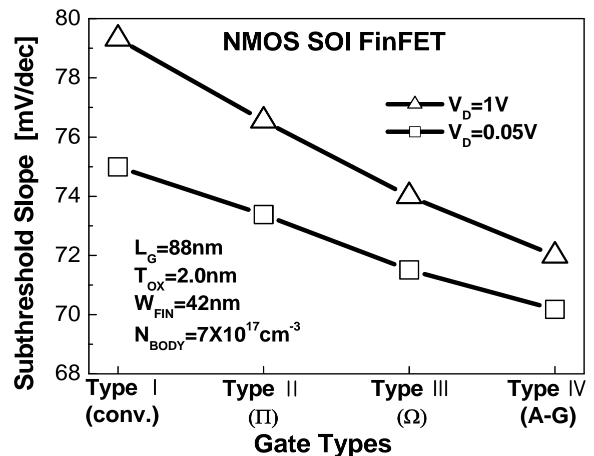


Fig.6 3-D simulated subthreshold slope for 4-types of structure. The gate structure evolves from Type I to Type IV, the subthreshold slope difference between V_D=0.05V and V_D=1V reduces.