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B-8-4 A Comprehensive Study of Hot-Carrier Effects in Body-Tied FinFETs

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ABSTRACT

Hot-carrier effects in body-tied FinFETs are investigated for the first time. Device degradation by hot-carrier injection (HCI) becomes significant as a fin width (channel thickness) increases. There are two competing conditions to degrade the device by HCI: V_G (<0.5V_{DD}) at I_{SUBmax} and V_G=V_D=V_{DD}. Interface trap generation is dominant at V_G at I_{SUBmax} and oxide trap are dominant at V_G=V_D=V_{DD}. At the narrow fin width, the device is more degraded by the interface trap generation (V_G at I_{SUBmax}) rather than by the oxide trap (V_G=V_D=V_{DD}). However, both mechanisms equally degrade the devices at the wide fin.

INTRODUCTION

FinFETs showed superior scalability for nano-scale CMOS with a simple fabrication process [1-2]. In the previous fully-depleted SOI FinFETs [3], the major difficulty was in finding the worst hot-carrier stress because a substrate current (I_{SUB}) can not be measured due to its floating body. In this work, hot-carrier-injection (HCI) effects were carefully studied at the conditions: V_G@I_{SUBmax} and V_G=V_D for various fin widths. It is well known that trap generation at Si-SiO_2 interface leads the device degradation at V_G@I_{SUBmax} (V_G/V_D~0.5), and trapped charges inside the gate oxide governs the device reliability at high V_G (V_G/V_D~1) in planar bulk-MOSFETs. To find the condition maximizing I_{SUB}, the ratio of V_G/V_D was measured for different fin widths. The mechanism of device degradation was investigated in terms of stress condition dependence and fin width dependence for the first time. This study can give us impact on determining the worst hot-carrier stress condition in SOI FinFETs, which show more robustness to short-channel effects and a superior scalability.

EXPERIMENTS

The process details were reported elsewhere [2]. A schematic of the body-tied FinFET is shown in Fig. 1. The gate length is 100nm, the fin widths are in the range of 20nm to 100nm, and the gate oxide thickness is 1.7nm. A threshold voltage (V_T) was read at 100nA of drain current at V_D=50mV, and on-state current (I_{ON}) was measured at V_G-V_T=1V and V_D=1V as key device parameters. All measured data are from n-channel FinFETs.

RESULTS AND DISCUSSIONS

Fig. 2 shows the typical bell-shaped I_{SUB}, which depends on the fin width (W_{Fin}) in the body-tied FinFETs. Beyond a critical V_G to cause I_{SUBmax}, I_{SUB} is effectively suppressed by the high gate field at the narrow fin whereas it is not sufficiently diminished at the wide fin. As the fin width increases, I_{SUBmax} becomes large, and V_G/V_D ratio at I_{SUBmax} becomes close to 1 as shown in Fig. 2 and Fig. 3. Fig. 4 represents an impact ionization rate, I_{SUB}/I_D [4]. It is large at the wide fin, which is consistent with the previous report [3]. The device degradation by HCI is more significant at the wide fin. Because, as V_G increased, I_{SUB}/I_D is not quickly suppressed at the wide fin than at the narrow fin. A saturated drain voltage (V_{Dsat}) was measured and plotted to V_G for various fin widths in Fig. 5. It is large at the narrow fin. Since the maximum lateral channel field is expressed as $E_m = (V_D - V_{Dsat})/l$, the impact ionization rate, which is a strong exponential function of E_m, is decreased due to large V_{Dsat} at the narrow fin. In addition to I_{SUB}, I_G is measured as well in Fig. 6. It is large at the wide fin, which shows the same trend as the previous report [5]. To find the worst case hot-carrier stress condition, I_{SUB} and I_G are measured and compared at both V_G@I_{SUBmax} and V_G=V_D on the same plot for various fin widths in Fig. 7. I_{SUB} quickly reduces at V_G=V_D as the fin width decreases, however, I_{SUB} is weakly depending on the fin width at V_G @I_{SUBmax}. I_G rapidly decreases as the fin width reduces at V_G@I_{SUBmax} while I_G is insensitive to the fin width at V_G=V_D. Discrepancy between both conditions tends to be zero at the wide fin. So, both of the interface trap generation and the oxide trapped charges deteriorate the device reliability equally at certain wide fin with. But, at narrow fin width, V_G@I_{SUBmax} and V_G=V_D are competing which condition degrades the device by HCI more.

It is crucial to determine the worst hot-carrier stress condition at the narrow fin because a worst degradation mechanism is unclear. But, it is less crucial to find the worst stress condition at the wide fin because both mechanisms equally affect the device degradation. To verify which is the worst hot carrier stress condition and to compare hot carrier immunity with the fin width, hot carrier stress was conducted with two competing conditions at W_{Fin}=20nm and W_{Fin}=70nm. Fig. 7 shows that I_{ON} degrades by HCI as the stress time increases for the different stress conditions as well as the two fin widths. Degradation of I_{ON} is always large at the wide fin with both stress conditions. Either stress condition equally degrades I_{ON} at the wide fin. At the narrow fin, it is worthwhile to note that the reduction of I_{ON} is larger at V_G@I_{SUBmax} than at V_G=V_D, and difference of I_{ON} between two conditions becomes increasing. This suggests that the interface trap generation lead the hot-carrier induced device degradation at the narrow fin with the stress condition, V_G @I_{SUBmax}. Fig. 9 shows threshold voltage (V_T) degradation for various drain voltages after 10,000 second stress. It duplicates the same scenario, which is similar to the trend in I_{ON} degradation.

CONCLUSIONS

In this work, the hot-carrier effects of the body-tied FinFETs are comprehensively studied for various stress conditions for the first time. It is observed that V_G/V_D ratio at I_{SUBmax} becomes large and I_{SUB} increases as the fin width broadens. I_G is also found to be increased as the fin width increases. At the narrow fin, the device degradation is led by the interface trap generation mechanism at the condition, V_G to cause peak I_{SUB}. At the wide fin, however, the oxide trapped charges at V_G=V_D condition and the interface trap generation at V_G@I_{SUBmax} are equally important. This work provides insight on finding the worst stress conditions to affect the hot-carrier induced device degradation in the SOI FinFETs.

ACKNOWLEDGEMENT

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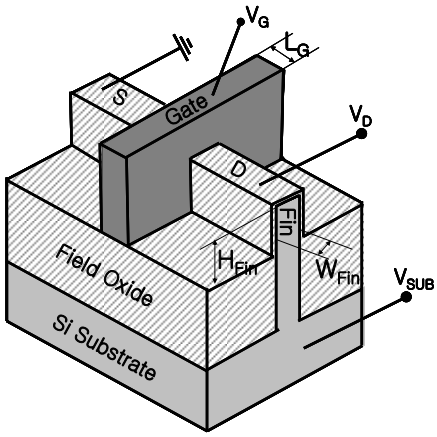

Fig.1 A schematic device structure of the body-tied FinFET (L_G=100nm, W_{Fin}=20, 40, 70, 100nm, T_{OX}=1.7nm).

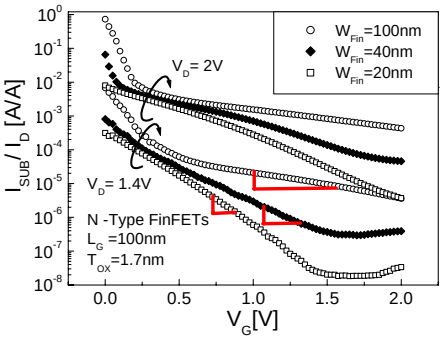

Fig.4 The impact ionization rate (I_{SUB}/I_D) is always small at the narrow fin. I_{SUB} is effectively suppressed as gate voltage increases at the narrow fin as well.

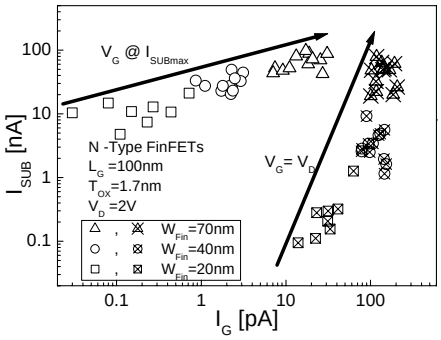

Fig.7 I_{SUB} increases quickly and I_G increases slowly as the fin width increases at V_G=V_D. The opposite trend is observed at V_G@I_{SUBmax}.

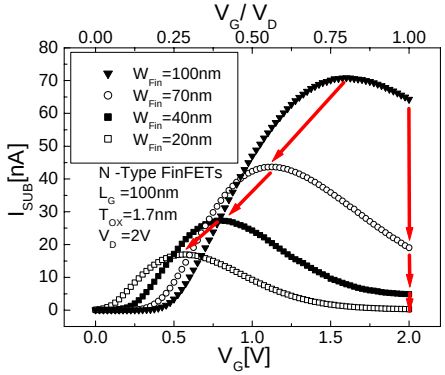

Fig.2 Typical bell-shaped I_{SUB} characteristics. V_G/V_D ratio to cause peak I_{SUB} increases, and I_{SUB} becomes large as the fin width widens.

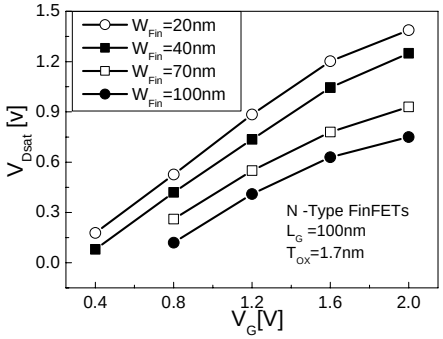

Fig.5 V_{Dsat} is large at the narrow fin, which results in reducing E_m, and suppressing impact ionization induced device degradation.

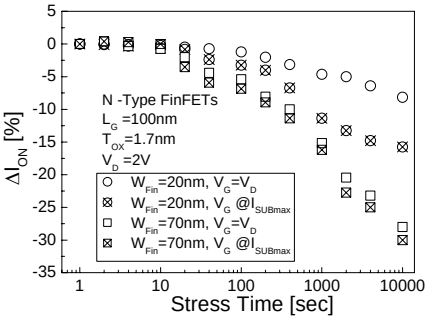

Fig.8 I_{ON} decreases as the stress time increases. It is more degraded at the wide fin and at V_G@I_{SUBmax}.

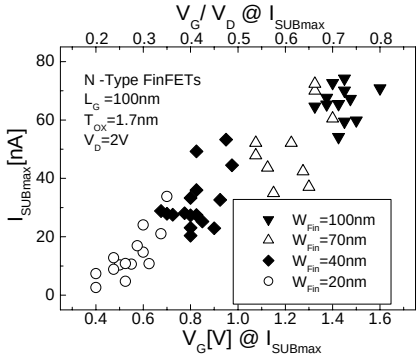

Fig.3 I_{SUBmax} becomes large as the fin width widens. And V_G/V_D ratio to cause I_{SUBmax} tends to unity as the fin width increases.

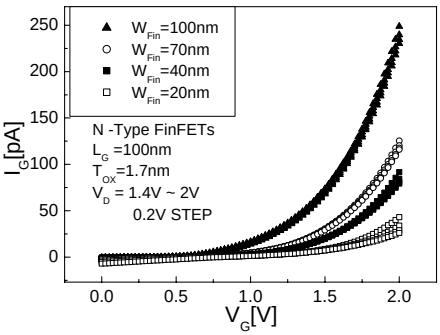

Fig.6 I_G becomes large as the fin width increases.

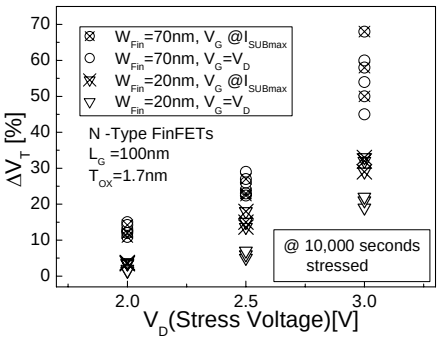

Fig.9 V_T increases as the stress voltage increases. Similar trend is found as Fig., too.