Molybdenum-Gate HfO_2 CMOS FinFET Technology

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Abstract

CMOS FinFETs with molybdenum gate and HfO_2 gate-dielectric are reported. By tuning the gate work function via nitrogen implantation and employing a narrow fin width, low values of threshold voltage (0.28/-0.17 V) and sub-threshold swing (67.5/62.5 mV/dec) were achieved. The use of HfO_2 rather than SiO_2 as the gate dielectric reduces the gate leakage current density by several orders of magnitude, for EOT in the range 1.75-1.95 nm. The observed weak temperature dependence for both electron and hole mobilities ($\mu_{eff} \sim T^{-0.95}$) is ascribed to soft phonon scattering.

Introduction

The double-gate FinFET is one of the most promising transistor structures for scaling CMOS technology to sub-10 nm gate lengths [1]. Integration of metal gate and high-k gate dielectric is desirable to reduce the equivalent gate-oxide thickness (EOT) while maintaining low gate leakage current, to improve transistor drive current and to relax the fin-width requirement for controlling short-channel effects [2-4]. In order to maximize carrier mobilities and avoid statistical dopant fluctuation effects on threshold voltage (V_T), the body of a FinFET should be undoped; V_T adjustment must be achieved by tuning the gate work function, in this case. Molybdenum (Mo) is a candidate gate material for future FD-SOI CMOS technology, because it is compatible with a standard CMOS process flow and its work function can be adjusted within the desired range (4.5-5.0 eV) via nitrogen implantation [5-7]. In this paper, the tunability of the Mo gate work function on HfO_2 is demonstrated for the first time using FinFETs.

Device Fabrication

Figure 1 outlines the FinFET process flow. UNIBOND® wafers were used as the starting substrates, and oxidized to reduce the SOI thickness to 50 nm. 80-nm wide Si fins were then defined by spacer lithography, while the source/drain (S/D) contact regions were defined by photolithography [8]. After patterning of the SOI and NH_3 pretreatment of the Si fin (110) sidewall surfaces, HfO_2 was deposited by CVD using Hf t-butoxide ($Hf(OC(CH_3)_3)_4$) as a precursor at 500°C. A 60 nm-thick Mo film was then deposited by DC magnetron sputtering with a plasma charge trap (PCT) to minimize sputtering damage [9]. For some n-channel FinFETs, nitrogen (1×10^{16} cm^{-2}, 5 keV) was implanted into the Mo gate film at 30° tilt on each side of the Si fins (*i.e.*, 60° tilt on the normal to the Mo gate surface) in order to reduce the effective Mo work function and achieve low V_T. The use of a low-energy tilted implant prevents nitrogen penetration into the underlying gate dielectric (Figure 2). The Mo was capped with *in-situ* n+ doped poly-Si and planarized by CMP. After gate patterning and S/D ion implantation, a 900°C 60s RTA in N_2 was used to activate the dopants. Finally, the devices were annealed at 400°C in forming gas. Figure 3 is a tilted-view SEM image of a completed FinFET. It should be noted that no metallization or silicided S/D structure was used in this study. Figure 4 shows a cross-sectional TEM image, and a close-up view of the gate stack at the Si fin sidewall. The Mo gate layer is continuous at the bottom of the Si fin due to the improved step-coverage with PCT sputtering [9].

Results and Discussion

A. Work Function Tuning of Mo Gate on HfO_2

Figure 5 compares measured I_D-V_{GS} characteristics for Mo-gate HfO_2 n-channel FinFETs with and without nitrogen gate implantation. It can be seen that V_T (defined as the gate voltage when I_D=100 nA/μm for V_{DS}=50 mV) is shifted from 0.73 V down to 0.28 V by the nitrogen implant. This indicates that the Mo-gate work function was effectively reduced by the nitrogen implant. Compared to our previous reports [5-7], the sub-threshold swing is greatly improved due to the minimization of Mo gate sputtering damage and the low-energy tilted nitrogen implantation [9]. The amount of reduction in gate work function is proportional to the nitrogen implant dose (Figure 6), but it is less for Mo on HfO_2 than for Mo on SiO_2 due to the Fermi-level pinning effect [10,11] and nitrogen diffusion into the HfO_2.

Figure 7 shows measured I_D-V_{GS} and I_D-V_{DS} characteristics for n-channel (with nitrogen-implanted Mo gate) and p-channel (with pure Mo gate) FinFETs. The V_T and sub-threshold swing values for the n-channel (p-channel) device are 0.28 (-0.17) V, and 67.5 (62.5) mV/dec, respectively. The p-channel

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device exhibits higher parasitic resistance than the n-channel device due to differences in p-type vs. n-type dopant redistribution in thin SOI during RTA [12].

Figure 8 compares measured C_G-V_G data (circles) with quantum-mechanical simulation (lines) [13]. The multi-fin device structure is shown in the inset. Extracted EOT in inversion is 1.95 or 1.92 nm for n-channel or p-channel devices, respectively. Stretch-out in the measured C-V characteristic is seen for the n-channel device, but not for the p-channel device. This result indicates an asymmetrical distribution of interface traps (D_{it}) within the energy bandgap (*i.e.*, higher D_{it} above E_i) [14], which explains the larger sub-threshold swing of the n-channel FinFET (Figure 7). As shown in Figure 9, the deviation from the ideal C-V characteristic is larger for a nitrogen-implanted Mo gate, indicating a higher interfacial trap density. This is likely due to the formation of an interfacial HfO_xN_y layer at the Si surface [15].

B. Carrier Mobility

Figure 11 shows the field-effect electron mobility for (110) Si sidewall Mo/HfO_2 FinFETs with (lines) and without (symbols) correcting for interface trap density [16]. The apparent electron mobility is lower for the nitrogen-implanted device as compared to the unimplanted device, due to the higher interface trap density. Figure 12 shows the field-effect hole mobility for a (110) Si sidewall Mo/HfO_2 FinFET. Both the electron mobility and the hole mobility are significantly degraded compared to the universal mobility curves for a (110) Si surface with SiO_2 gate dielectric [17]. In order to elucidate the reason for this, the carrier mobility dependence on temperature (in the range from -50°C to 200°C) was investigated. Both electron and hole mobilities increase with decreasing temperature due to reduced phonon scattering (Figure 13). However, at low field strength (0.1 MV/cm for electrons and 0.2 MV/cm for holes) they exhibit a weaker temperature dependence ($\mu_{eff} \sim T^{-0.95}$) compared to mobilities for SiO_2 gate dielectric ($\mu_{eff} \sim T^{-1.5}$), as shown in Figure 14. This indicates that the mobilities are limited by HfO_2 soft phonon scattering [18,19]. Figure 15 shows that the peak electron mobility achieved in this work is comparable to previously published data for (100) Si with HfO_2 gate dielectric. This is notable because the electron mobility is lower for a (110) Si surface than for a (100) Si surface, with SiO_2 gate dielectric.

C. HfO_2 Gate Dielectric

Figure 16 shows the measured gate leakage current density characteristics. Lower gate leakage is seen for the p-channel FinFET as compared to the n-channel FinFET (unimplanted Mo gate), due to the larger hole barrier height for HfO_2 [20]. Compared to a SiO_2/poly-Si gate stack, the gate leakage current is reduced by 3-4 orders of magnitude for the same EOT (Figure 17). The nitrogen-implanted Mo-gate n-channel FinFET shows increased gate current, likely due to nitrogen diffusion into the HfO_2 which degrades the interfacial and bulk properties of HfO_2 [15]. Deuterium annealing is effective to reduce the gate current by 1-2 orders of magnitude (Figure 16), and to improve the effective electron mobility slightly (Figure 19). This implies that deuterium can effectively passivate traps within HfO_xN_y. Figure 20 shows the gate dielectric charge-to-breakdown (Q_{BD}) characteristics under constant voltage stressing. These initial results indicate that the reliability of a nitrogen-implanted Mo-gate device is comparable to that of a pure Mo-gate device. Key results are summarized in Table I.

Summary

CMOS FinFETs with Mo gate on HfO_2 are demonstrated for the first time. Low gate leakage current density was achieved for a thin inversion EOT (down to 1.72 nm), with carrier mobilities comparable to previously reported works (limited by soft phonon scattering). V_T adjustment is shown to be feasible by tuning the effective Mo work function via nitrogen implantation. Further process optimization is needed to prevent nitrogen diffusion into the HfO_2, to make Mo-gate HfO_2 FinFET technology suitable for future nanoscale CMOS technology.

Acknowledgement

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- o Fin formation (LTO spacer lithography)
- o Sacrificial oxidation (900C 3min dry O_2)
- o Diluted HF wet etching
- • **NH_3 pre-treatment**
- • **CVD HfO_2 deposition**
- • **Mo deposition (60nm)** (DC magnetron sputtering w/ PCT)
- • **Nitrogen implantation** (NMOS split) (5 KeV 1×10^{16} cm^{-2} 30° tilt)
- o *In-situ* N+ poly-Si deposition (400nm)
- o Chemical Mechanical Polishing
- o LTO deposition
- o Gate formation
- o n+/p+ S/D implantation (0° tilt)
- o RTA activation (900C 60s N_2)
- o Forming gas annealing (split)

Fig.1 Process sequences for Mo/HfO_2 FinFETs.

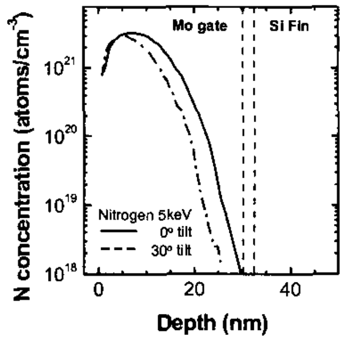

Fig.2 Simulated implanted nitrogen profiles in the Mo/HfO_2 stack (dose = 5×10^{15} cm^{-3}).

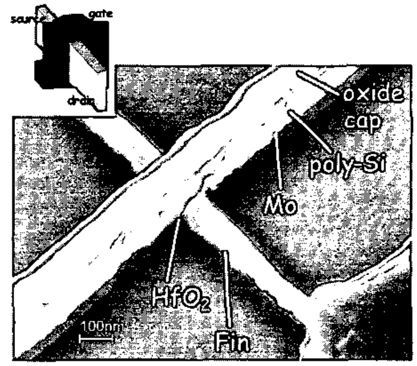

Fig.3 Tilted-view SEM image of Mo/HfO_2 FinFET.

Fig.4 (a) Cross-section TEM image and (b) close-up of Mo-gate and HfO_2 interface after 900C 60s in N_2 ambient. The Mo gate was implanted with nitrogen to a dose of 1×10^{16} cm^{-2}.

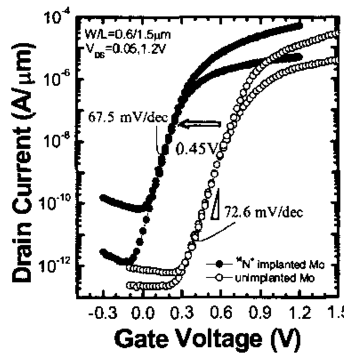

Fig.5 Nitrogen implantation into Mo is effective for V_T control without degrading sub-threshold swing.

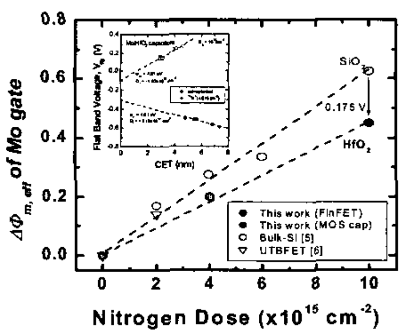

Fig.6 Change in effective gate work function *vs.* nitrogen implantation dose.

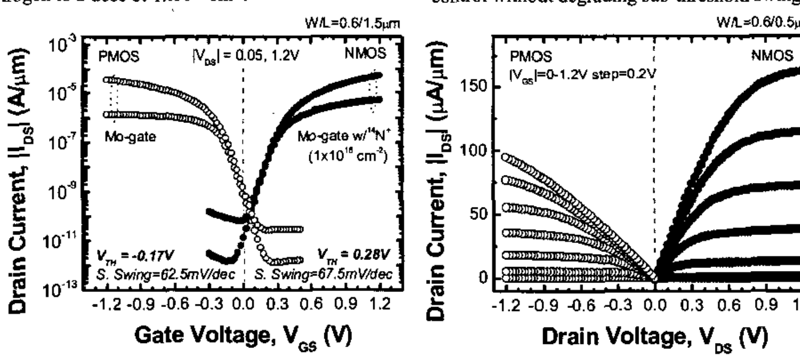

Fig.7 Measured I_D-V_{GS} and I_D-V_{DS} characteristics of CMOS FinFETs. Low energy (5 KeV) and 30° tilted nitrogen implantation has been applied to the Mo gate for the n-channel FinFET.

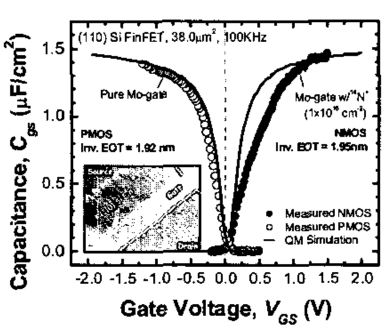

Fig.8 Measured C_G-V_G characteristics for n-channel and p-channel Mo/HfO_2 FinFETs.

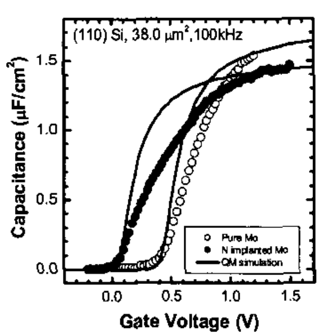

Fig. 9 Comparison of n-channel C_G-V_G characteristics with and without nitrogen implantation.

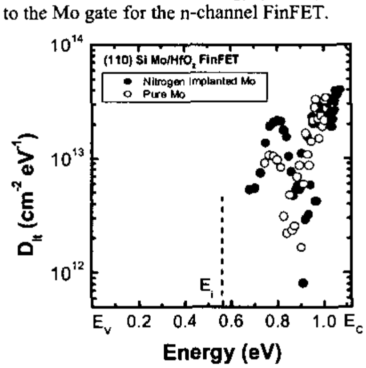

Fig.10 Extracted interface trap density for pure (○) and N-implanted (●) Mo/HfO_2

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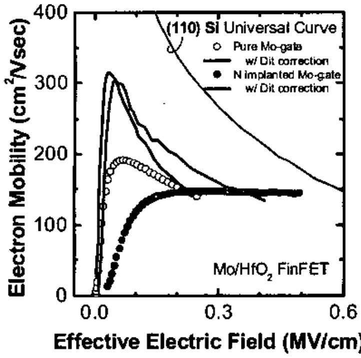

Fig.11 Effective electron mobility for (110) n-channel Mo/HfO_2 FinFETs with and w/o correcting for D_{it}.

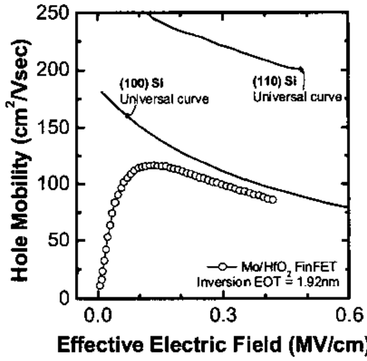

Fig.12 Effective hole mobility for (110) p-channel Mo/HfO_2 FinFET.

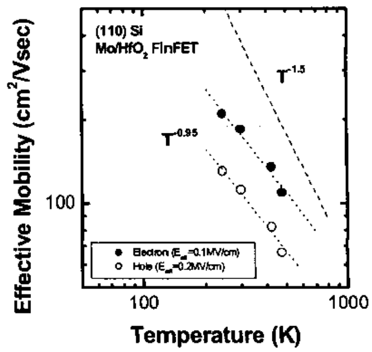

Fig.14 Electron and hole mobilities for HfO_2 FinFETs show weaker dependence on temperature, than for SiO_2 ($T^{-1.5}$) devices.

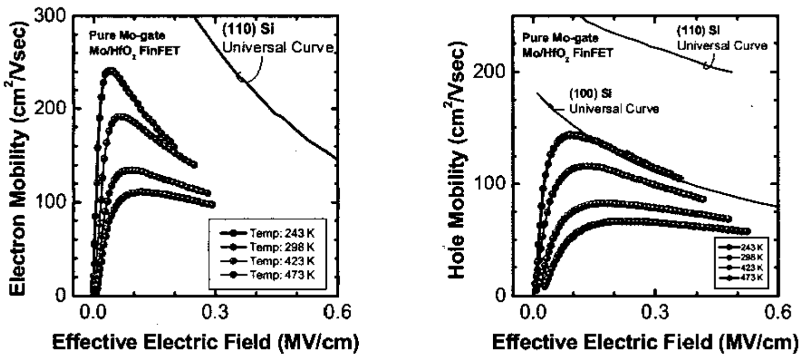

Fig.13 Effective (a) electron and (b) hole mobility at various measurement temperatures.

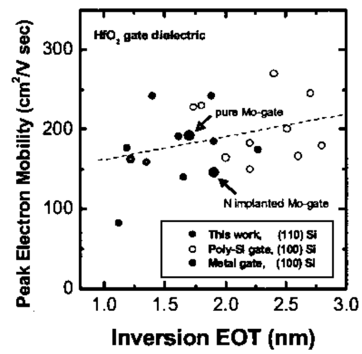

Fig.15 Peak electron mobility *vs.* inversion EOT.

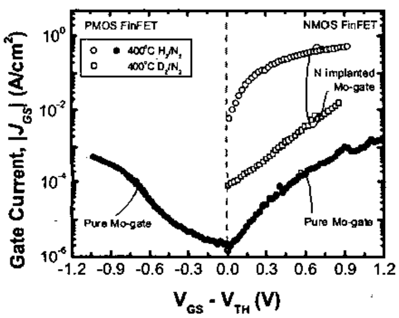

Fig.16 Gate leakage current characteristics for n- and p-channel Mo/HfO_2 FinFETs. D_2 annealing is effective to reduce I_{gate}.

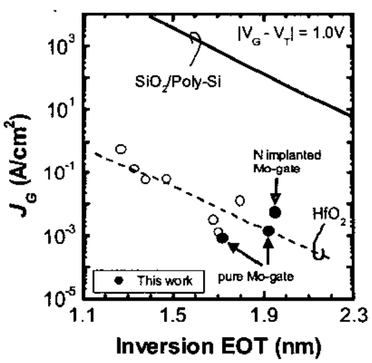

Fig.17 EOT (inversion) *vs.* gate leakage current.

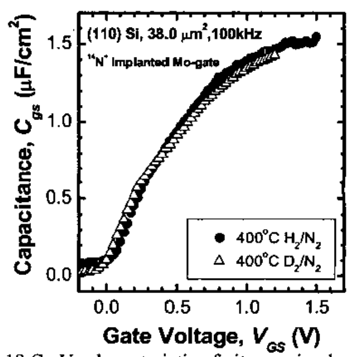

Fig.18 C_G-V_G characteristic of nitrogen implanted Mo gate device for different forming gas annealing.

Table I. Key device results of Mo/HfO_2 FinFETs

	NMOS		PMOS
	Low V_T	High V_T	Low V_T
$^{14}N^+$ implant (cm^{-2})	$1x10^{16}$	-	-
Measured V_T (V) (@100nA/μm)	0.28	0.73	-0.17
S. Swing (mV/dec)	67.5	72.6	62.5
Inv. EOT (nm)	1.95	1.75	1.92
Jgate (mA/cm^2)	5.55	0.86	0.52
Peak mobility (cm^2/V sec)	146.7	191.9	115.9

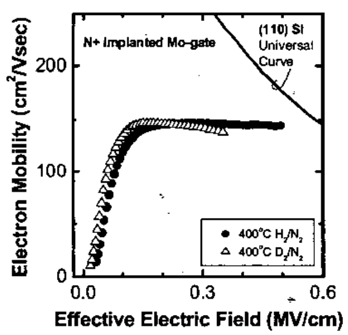

Fig.19 Effective electron mobility for different forming gas annealing.

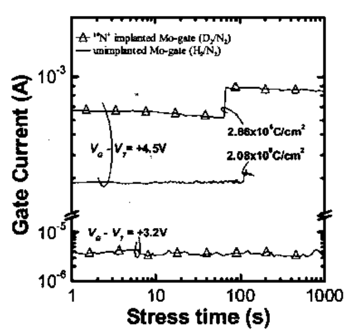

Fig.20 Gate dielectric breakdown characteristic for n-channel Mo/HfO_2 FinFET