Sub-Lithographic Nanofabrication Technology for Nanocatalysts and DNA Chips

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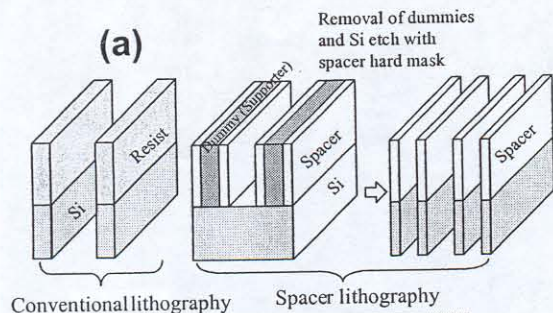
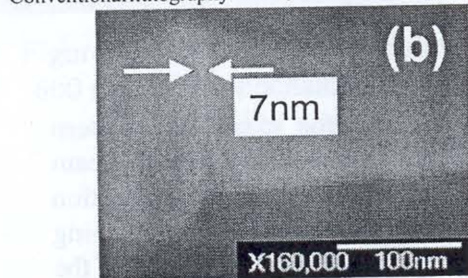
We describe a spacer lithography, parallel process for nanometer pattern generation on a wafer scale with resolution comparable to the best electron beam lithography pattern. The essence of the technique is based on the conformal deposition of material during LPCVD process. By depositing a material that has a different etching property than the sacrificial layer and directionally etching the material on the top of the step, the sacrificial layer can then be removed selectively, leaving only the material deposited on the sidewall (spacer) as shown in Fig. 1(a). The feature size thus generated is determined by the thickness of the deposited material, not by the photolithography. Since the thickness of the deposited film can be controlled to 10 nm or less with high precision, this method is capable of generating sub-10 nm patterns as shown in Fig. 1 (b). Repeating this process and alternating the sidewall and sacrificial materials, dense nanowires with sub-100 nm spacing can be fabricated on a wafer scale as shown in Fig. 1 (c). This method can be used to pattern silicon fins for double-gate MOSFETs (FinFETs) [1]. We have also investigated the fabrication of nanowire catalysts using this technique to fabricate a template for nanoimprint lithography, followed by Pt lift-off patterning as shown in Fig. 2. Catalytic properties of these structures are currently under investigation.

This technique is also used to make gap-like patterns. A first poly-Si layer is deposited and patterned by standard photolithography. Then, thin CVD oxide is deposited and etched back. Sidewall spacer oxide is left along the first poly-Si structure. After another thick ploy-Si deposition and chemical-mechanical polishing, two planarized poly-Si electrodes are formed with a thin, vertical CVD oxide in between. The oxide serves as sacrificial layer. After release of this oxide by HF wet etching, a sub-50nm gap is formed as shown in Fig. 3. This structure has been used for label free DNA hybridization detection by measuring the change in dielectric capacitance. Fig. 4 shows that the capacitance increases more rapidly after hybridization than before hybridization as the input frequency decreases when conjugated DNA base pairs (G-C) are made. However, there is no significant difference of the measured capacitance between before and after hybridization in the case of non-conjugated DNA strands. Similar behavior was also observed in T-A pairs. Due to the full compatibility with silicon microfabrication technology, DNA chips without any requirement of label process is feasible so that it reduces cost and dramatically speed up assay of DNA hybridization.

References

[1] Y.-K. Choi, et al., "Sub-20nm CMOS FinFET Technologies", *IEEE IEDM Technical Digest,* p.421-24, 2001.





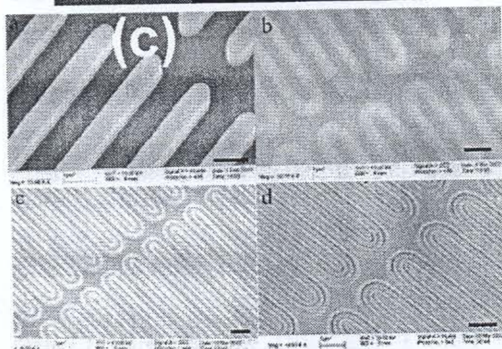


Fig. 1. Schematic view and SEM photographs by spacer lithography. (a) Minimum sized features are defined by spacers, (b) SEM photograph of 7nm Si nanowire defined by spacer lithography, and (c) multiplicated nanowires by repeating spacer lithography (line width=70nm, space=80nm in d).

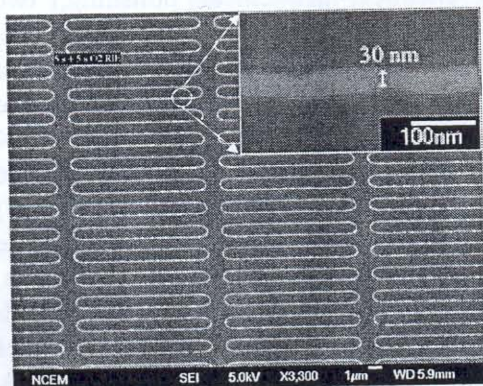
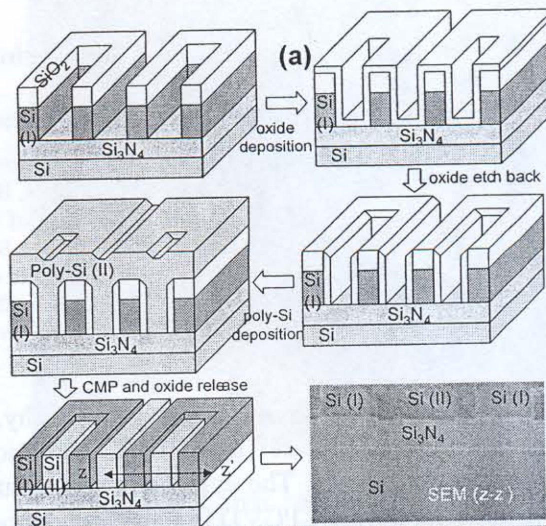


Fig. 2. SEM photographs of Pt line-like catalysts. Pt nanowires are fabricated by nanoimprint lithography with Si mold made by one time spacer lithography and Pt lift-off.



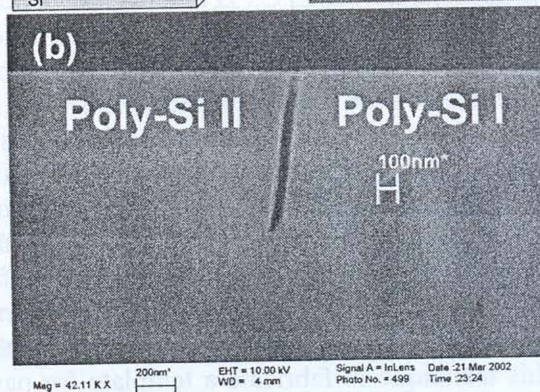


Fig. 3. Process flow of nanogaps (a) and cross-sectional SEM photographs (b). The gap width is determined by the deposited oxide film thickness.

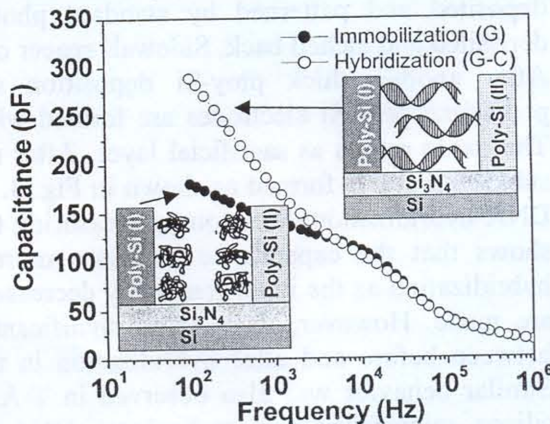


Fig. 4. Measured capacitance versus input frequency after immobilization and hybridization. Capacitance increase as the frequency decreases in the conjugated base pairs (G-C) and there is no significant difference of capacitance in the non-conjugated base pairs (G-T).