NANOSTRUCTURED ELECTRODES FOR NEURAL CHIP APPLICATIONS

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Abstract

For the analysis of cultured neural networks and cells in on-chip biosensors, microelectrodes must be optimized for impedance and selectivity. We present a new method of increasing the effective electrode surface for decreased impedance. Here, high aspect ratio pillar-like polysilicon nanostructures are created in a reactive ion etch. The pillars are 0.3 μm in height and less than 100 nm in diameter. When compared to a control substrate, these nanostructures increase the surface area by 12-15 times and result in an order of magnitude decrease in impedance.

Keywords: nanostructures, impedance, microelectrode

1. Introduction

The interface between neurons and electrodes is one of the key issues in implantable microdevices or on-chip bioelectronics. The ideal electrode has maximum selectivity and minimum impedance. Selectivity refers to the ability to select a single neuron from a multitude of interconnected cells. High electrode impedance attenuates and filters the measured signal. In addition, a sufficient signal-to-noise ratio is required for data analysis; low electrode impedance gives high signal gain [1]. However, an increase in electrode selectivity with smaller geometric electrode size results in increased impedance and noise. To optimize the electrode, the impedance per unit of geometric surface area must be decreased by altering its nanostructure. Because the total electrode impedance is approximately proportional to the effective surface area, a 10 times increase in surface area should give an order of magnitude decrease in impedance [2]. Applications of these nanostructures extend beyond electrodes, because they may improve integration of tissue with an implanted microdevice as cells anchor onto the increased surface area that they provide.

2. Nanostructure Fabrication

The substrate is a 1 μm film of heavily n-type in-situ doped polysilicon, which was deposited by low pressure chemical vapor deposition (LPCVD) onto a quartz wafer. Electrode pads are defined by conventional I-line lithography and a two-step anisotropic plasma etch (Lam Research 9400 TCP): a breakthrough step removes the native oxide and an etch step patterned the polysilicon (Fig.1). After stripping the photoresist, nano-pillars are formed on the electrodes, also by using a two-step anisotropic plasma etch (Fig.2). The density and diameter of the nano-pillars is controlled by the ratio of HBr and O_2. A larger HBr:O_2 ratio is etch dominant, while a smaller HBr:O_2 ratio is passivation dominant and gives more densely packed nanostructures.

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In this device, an array of nanostructured electrodes in the center of the substrate are connected to polysilicon lines which lead out to bond pads at the edge (Fig. 3a). The electrodes at the center are squares with widths of 20, 50, 100, and 200 µm. A 35 mm diameter tissue culture dish with the bottom drilled out was glued to the quartz substrate using 100% silicone adhesive (Fig. 3b). The bond pads are ultrasonically bonded to hand-made connectors for data collection.

3. Experimental

Impedance was measured from the electrodes at 1 kHz (Fig 4). The nanostructures increase the surface area by 12-15 times and result in an order of magnitude decrease in impedance.

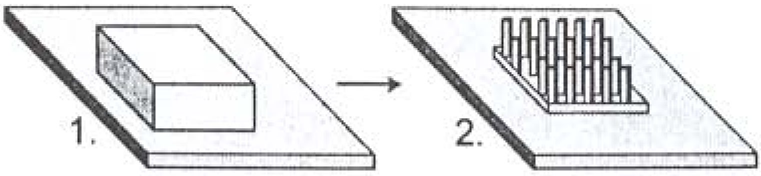

Fig. 1. Nanostructure fabrication.

1. A polysilicon film is deposited on a quartz wafer and patterned.
2. The film is etched back in a highly selective reactive ion etch, which produces the nanostructures.

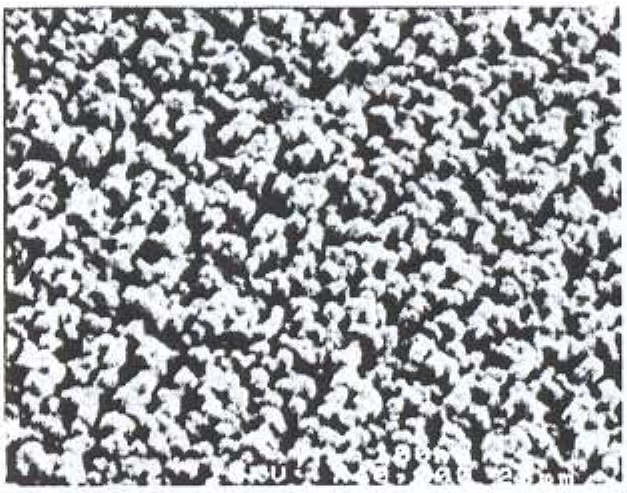

Fig. 2. The nanostructures are less than 100 nm in diameter.

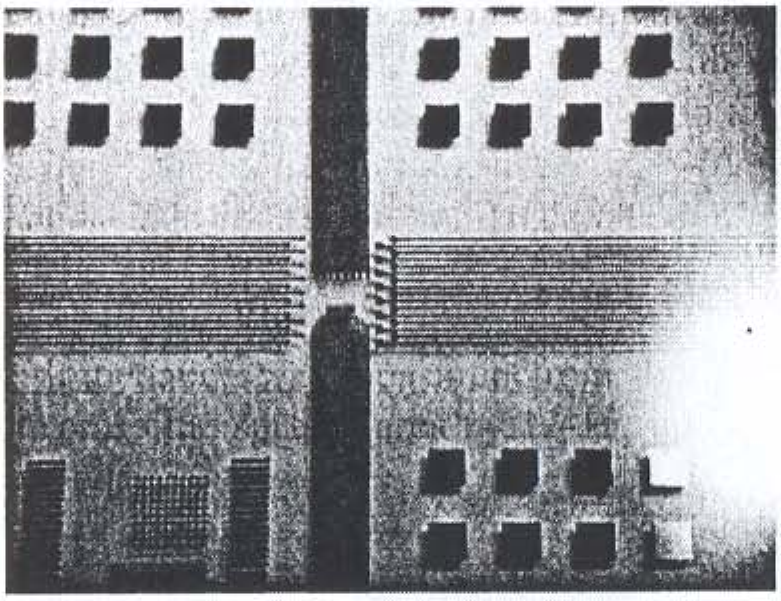

Fig. 3.(a) An array of electrodes in the center are connected to polysilicon lines.

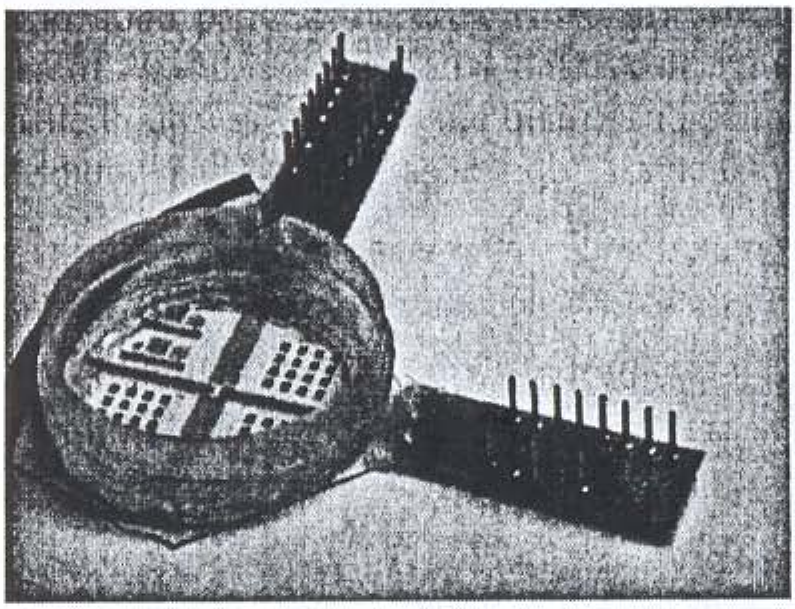

Fig. 3.(b) View of the entire assembly.

4. Results and discussion

High aspect ratio pillar-like polysilicon nanostructures were fabricated. Their diameters ranged from 20 to 100 nm; diameter and packing density are controlled by the ratio of HBr and O_2 in a highly selective silicon RIE. The nanostructures decrease the impedance by an order of magnitude.

Table 1. Nanostructure etch gas ratio affects the final surface area ratio

Wafer	*Nanostructure etch gas ratio*	*Surface area ratio*
Control	-	1
1	200 HBr : 6 O_2	12.5
2	200 HBr : 9 O_2	15

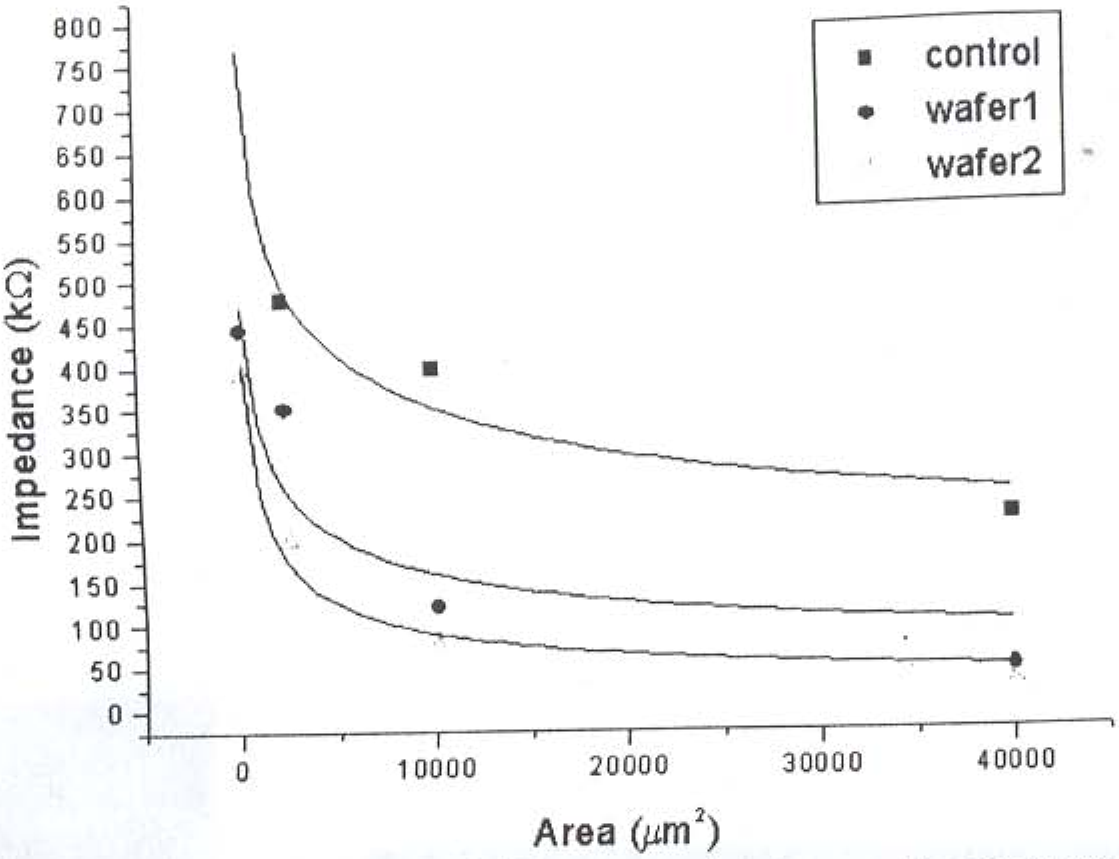

Fig. 4. Impedance recordings. Wafers 1 and 2 have nanostructures on the electrode pads. The nanostructures decrease the impedance by an order of magnitude.

5. Conclusions

High aspect ratio pillar-like polysilicon nanostructures were fabricated. The nanostructures increase the surface area by 12-15 times and result in an order of magnitude decrease in impedance. More studies are necessary in which these electrodes are used to record neural signals.

Acknowledgements

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References

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