ADVANCED MATERIALS AND PROCESSES FOR NANOMETER-SCALE FINFETS

Tsu-Jae King, Yang-Kyu Choi, Pushkar Ranade^ and Leland Chang

Electrical Engineering and Computer Sciences Dept., ^Materials Science and Engineering Dept.
University of California at Berkeley
Berkeley, California 94720-1770 USA

Abstract -- *This paper discusses the need for advanced materials and processes to maximize the performance benefit of the FinFET for sub-50-nm CMOS technologies. Recent work to develop a tunable work-function gate technology and low-thermal-budget source/drain contact process are reviewed.*

INTRODUCTION

Advanced transistor structures such as the ultra-thin-body (UTB) MOSFET [1] and the double-gate MOSFET [2] are more scalable than the classical bulk-Si structure and hence are likely to be adopted for the manufacture of CMOS integrated circuits beyond the 50-nm-technology node [3]. The quasi-planar FinFET (Figure 1) offers the superior scalability of a double-gate MOSFET structure together with a process flow and layout similar to that of the conventional MOSFET [4]. Hence, it recently has been investigated by several groups [5]-[7]. In order for a FinFET technology to provide maximum performance benefit over bulk-Si MOSFET technology, advanced materials and processes are required. This paper discusses the advantages of tunable-work-function gate materials and raised source/drain contact processes for optimizing CMOS FinFET circuit performance.

GATE MATERIAL CONSIDERATIONS

Impact of Gate Work Function on Performance

In a FinFET, short-channel effects can be effectively suppressed by using a thin body (narrow fin) rather than heavy channel doping. A lightly doped channel provides improved immunity to variations in threshold voltage (V_T) resulting from statistical dopant fluctuations, as well as enhanced carrier mobility for higher transistor drive current because of the lower transverse electric field in the inversion layer [8]. However, it requires that a means other than channel doping is available for adjusting V_T.

The proper value of V_T can be achieved in a lightly doped FinFET by employing dual n+/p+ poly-Si gates [6]. In this case, V_T is tuned by adjusting the relative thicknesses of the gate oxide and body (Figure 2) [9]. This approach makes V_T more sensitive to variations in body thickness, however. Also, it results in higher transverse electric fields which degrade transistor drive current and increase gate-induced drain leakage [10]. Symmetric gates are therefore preferred for optimal performance.

For lightly doped thin-body (fully depleted) SOI CMOS transistors, the required range of work functions for symmetric gates is 4.4-5.0 V (Figure 3) [11], which precludes doped poly-Si as a gate material. Metallic gate materials are therefore needed, and provide the additional advantage of eliminating the gate depletion effect for further improvement in transistor drive. Figure 4 compares the performance (fanout-of-4 inverter delay) of thin-body SOI CMOS technologies against that of bulk-Si CMOS technology, obtained through mixed-mode simulation using realistic device structures based on ITRS specifications [12]. For the cases of poly-Si gate (n+ poly-Si for NMOS, and p+ poly-Si for PMOS) and midgap-work-function gate, high channel doping is used to achieve the proper values of V_T. It can be seen that the use of an optimized metal gate technology in conjunction with light body doping for thin-body SOI transistors yields the best performance, by a significant margin.

Because of their disparate gate work function requirements, different gate materials must be employed for n-channel *vs.* p-channel lightly doped FinFETs. The simplest process integration approach is to deposit a single gate material and then to selectively modify its work function as needed, as is done for a conventional poly-Si gate technology. Researchers have recently found that the work function of a nickel silicide (NiSi) gate electrode can be either 4.6 V or 5 V, if the poly-Si starting material is heavily doped either n-type or p-type, respectively, prior to complete silicidation [13]. Thus, NiSi is a candidate for dual-work-function gate technology. Potential issues such as dopant penetration through thin gate oxide, changes in gate-oxide thickness (due to segregation of oxygen during the silicidation process), and thermal stability remain to be investigated, however. Molybdenum (Mo) is another candidate for dual-work-function gate technology, one which does not require the use of dopants for work function adjustment. The suitability of Mo as a gate electrode for CMOS FinFET application is discussed in the following subsection.

Molybdenum Gate Technology

Mo is an attractive candidate for gate-electrode application because of its excellent compatibility with CMOS processing, low resistivity [14] and a coefficient of thermal expansion that matches silicon. Its high work function (~5 V) makes it suitable as a gate material for p-channel FinFETs. The work function of Mo on SiO_2 can be lowered in a controllable manner by low-energy $^{14}N^+$ implantation followed by thermal annealing [15], to make it suitable as a gate material for n-channel FinFETs as well. From Figure 5, it can be seen that the Mo gate work function decreases with increasing implant dose and energy; it also increases with post-implant anneal temperature (T_{anneal}), saturating at ~4.4 V for T_{anneal}=900°C [16]. The mechanism for the reduction in work function is the segregation of N and formation of Mo_2N at the gate/gate-dielectric interface.

A tunable-work-function Mo gate technology recently has been successfully applied to p-channel FinFETs [17]. The capability to achieve multiple V_T values by selectively adjusting the $^{14}N^+$ implant dose (Figure 6) is important because it enables optimization of V_T for high-performance *vs.* low-power applications, without the need for channel doping. Care must be taken to optimize the Mo film thickness and implantation energy in order to avoid degrading the gate-oxide/Si-fin interface (Figure 7), however.

NARROW FIN FORMATION

Generally, the minimum gate length (L_g) on an IC chip is the smallest feature which can be defined by conventional lithographic processes. In order to suppress short-channel effects, the thickness of a lightly doped FinFET body (*i.e.* the fin width W_{fin}) must be ~1.5× smaller than the gate length, however [18]. Sub-lithographic fins (narrower than any feature which can be defined by conventional lithography) can be formed in an SOI film by using spacers, formed along the sidewalls of a sacrificial patterned layer, as a hard mask [19]. The spacers are formed by conformal deposition of the spacer material, followed by anisotropic etch to remove this material from the lateral surfaces on the wafer (Figure 8). The width of the spacers is determined by the thickness of the deposited spacer layer, and can be very uniform across a wafer (Figure 9) [19].

SOURCE/DRAIN CONTACT FORMATION

Parasitic resistance associated with the thin-body source and drain (S/D) regions can seriously limit transistor drive current, particularly for electrical channel lengths below 50 nm [6]. An optimized FinFET CMOS fabrication process should therefore provide for heavy and uniform doping of the thin-body (narrow-fin) S/D extensions, as well as selectively thickened S/D contact regions, to minimize parasitic resistance.

Tilted-Angle Source/Drain Ion Implantation

For any MOSFET, the S/D regions should be heavily doped uniformly across the entire width of the channel, to achieve low parasitic resistance with uniform electrical channel length (L_{eff}) for good control of short-channel effects. Since the FinFET is a vertical structure, the S/D dopants should thus be ideally implanted at a 90° angle to the fin, which is not practical for a manufacturing process. High-performance single-fin FinFETs have been fabricated with S/D implants performed at a relatively high tilt angle $\theta = 45^o$ [6]. Since multiple fins are required to achieve a wide-channel FinFET, there exists a tradeoff between θ and FinFET layout area: the spacing between fins ($S_{fin\text{-}to\text{-}fin}$) cannot be too small:

$$S_{fin\text{-}to\text{-}fin} \geq H_{fin} (\tan \theta) \qquad (1)$$

where H_{fin} is the height of the Si fin; otherwise, shadowing of the S/D implant will occur. In order to guarantee that the layout efficiency of a wide-channel FinFET will be no worse than that of a conventional bulk-Si MOSFET, the height of the fin should be greater than or equal to the fin pitch:

$$H_{fin} \geq W_{fin} + S_{fin\text{-}to\text{-}fin} \qquad (2)$$

Given the constraints in Equations (1) and (2), the S/D implant tilt angle is limited to less than 45°:

$$\tan \theta < 1 \qquad (3)$$

Therefore, it will be very difficult to achieve perfectly uniform L_{eff} throughout the height of a fin for optimal double-gate transistor performance with the FinFET structure.

Selective Thickening of Source/Drain Contact Regions

Parasitic resistance associated with the S/D contact regions can be reduced by selectively thickening the Si fin in these regions. Selective Si epitaxy has been successfully applied for this purpose [6]. Silicon-germanium (SiGe) alloys with moderate Ge content (less 50 atomic percent) can be selectively deposited onto Si by CVD and provide lower sheet resistance and specific contact resistivity (close to 10^{-8} Ω-cm^2) than can be achieved with Si [20]. Another significant benefit of SiGe is that lower annealing temperatures can be used to activate dopants, to alleviate stability issues for advanced gate-stack materials such as high-permittivity gate dielectrics and metallic gate electrodes. Pure Ge can be deposited selectively at low temperatures (<350°C) in a conventional LPCVD furnace, using GeH_4 as the gaseous source, to form the raised-S/D structure (Figure 10) [21]. This process has been successfully applied to improve I_{dsat} for sub-100nm FinFETs (Figure 11) [22]. Ultimately, parasitic S/D resistance should be minimized by further forming a silicide (or germanosilicide) in the thick S/D regions.

SUMMARY

Metallic gate-electrode materials and low-resistance S/D formation processes will be required in order for the FinFET to provide significant circuit performance advantages over the bulk-Si MOSFET in future sub-50-nm CMOS technologies. Mo gate technology shows promise for future FDSOI-CMOS application, particularly if multiple values of V_T are needed. Uniform S/D doping throughout the height of a fin in the S/D regions is desirable for good control of short-channel effects, but presents a technological challenge. Selective thickening of the S/D contact regions and subsequent silicidation will be necessary to achieve high drive current meeting ITRS specifications.

ACKNOWLEDGEMENTS

Fruitful discussions with Chenming Hu and Jeffrey Bokor are gratefully acknowledged. Ultra-low-energy N^+ implants (for the Mo gate study) were provided by Aditya Agarwal and Michael Ameen of Axcelis Technologies Inc. This work is supported under MARCO contract 2001-MT-887 and SRC contract 2000-NJ-850. The FinFETs were fabricated in the UC Berkeley Microfabrication Laboratory.

REFERENCES

[1] Y.-K. Choi *et al.*, "Ultrathin-body SOI MOSFET for deep-sub-tenth micron era," *IEEE Electron Device Letters*, (May, 2000), pp. 254-255.

[2] D. Frank *et al.*, "Monte Carlo simulation of a 30 nm dual-gate MOSFET: how short can Si go?" *IEDM Technical Digest*, (December, 1992), pp. 553-556.

[3] R. Chau *et al.*, "A 50 nm depleted-substrate CMOS transistor (DST)," *IEDM Technical Digest*, (December, 2001), pp. 621-624.

[4] N. Lindert *et al.*, "Sub-60-nm quasi-planar FinFETs fabricated using a simplified process," *IEEE Electron Device Letters*, (October, 2001), pp. 487-489.

[5] Y.-K. Choi *et al.*, "Sub-20nm CMOS FinFET tchnologies," *IEDM Technical Digest*, (December, 2001), pp. 421-424.

[6] J. Kedzierski *et al.*, "High-performance symmetric-gate and CMOS-compatible V_t asymmetric-gate FinFET devices," *IEDM Technical Digest,* (December, 2001), pp. 437-440.

[7] F.-L. Yang *et al.*, "35 nm CMOS FinFETs," *Symposium on VLSI Technology, Digest of Technical Papers,* (June, 2002), pp. 104-105.

[8] D.A. Antoniadis, "MOSFET scalability limits and "new frontier" devices," *Symposium on VLSI Technology, Digest of Technical Papers,* (June, 2002), pp. 2-5.

[9] S.H. Tang *et al.*, "FinFET -- a quasi-planar double-gate MOSFET," *International Solid-State Circuits Conference* (February, 2001).

[10] J.G. Fossum *et al.*, "Extremely scaled double-gate CMOS performance projections, including GIDL-controlled off-state current," *IEEE Transactions on Electron Devices*, (November 1999), pp. 2195-2200.

[11] L. Chang *et al.*, "Gate length scaling and threshold voltage control of double-gate MOSFETs," *IEDM Technical Digest*, (December, 2000), pp. 719-722.

[12] *International Technology Roadmap for Semiconductors*, 2001. http://public.itrs.net/Files/2001ITRS/Home.htm2001

[13] M. Qin *et al.*, "Investigation of polycrystalline nickel silicide films as a gate material," *Journal of the Electrochemical Society*, (May, 2001), pp. G271-G274.

[14] *VLSI electronics: microstructure science*, Vol. 9, Academic Press, New York, (1985), 477 p.

[15] P. Ranade *et al.*, "Work function engineering of molybdenum gate electrodes by nitrogen implantation," *Electrochemical and Solid-State Letters*, (November, 2001), pp. G85-G87.

[16] P. Ranade *et al.*, "Tunable-Work-Function Molybdenum Gate Technology for FDSOI-CMOS," *IEDM Technical Digest*, (December, 2002).

[17] Y.-K. Choi *et al.*, "FinFET Process Refinements for Improved Mobility and Gate Work Function Engineering," *IEDM Technical Digest*, (December, 2002).

[18] N. Lindert *et al.*, "Quasi-planar NMOS FinFETs with sub-100nm gate lengths," *59th Device Research Conference, Conference Digest*, (June, 2001), pp. 26-27.

[19] Y.-K. Choi *et al.*, "Spacer FinFET: Nano-scale CMOS technology for the terabit era," *2001 International Semiconductor Device Research Symposium Proceedings*, (December, 2001), pp. 543-546.

[20] S. Gannavaram *et al.*, "Low temperature (≤800°C) recessed junction selective silicon-germanium source/drain technology for sub-70 nm CMOS," *IEDM Technical Digest*, (December, 2000), pp. 437-440.

[21] P. Ranade *et al.*, "Application of silicon-germanium in the fabrication of ultra-shallow extension junctions for sub-100 nm PMOSFETs," *IEEE Transactions on Electron Devices*, (August, 2002) pp. 1436-1443.

[22] N. Lindert *et al.*, "Quasi-planar FinFETs with selectively grown germanium raised source/drain," *2001 IEEE International SOI Conference Proceedings*, (October, 2001), pp. 111-112.

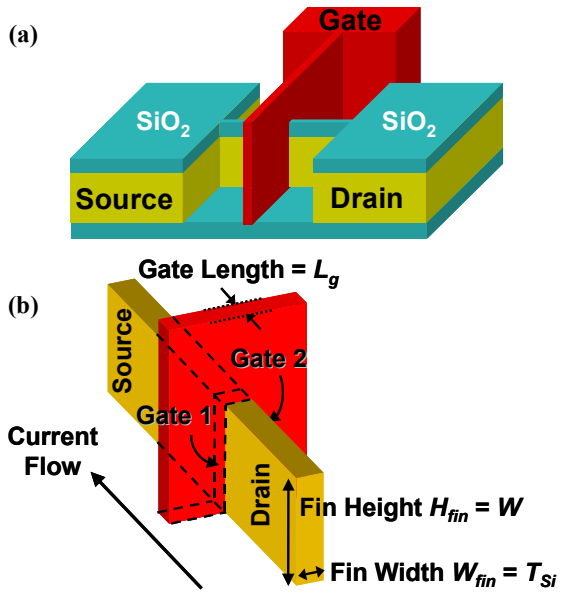

Figure 1: **(a)** Quasi-planar FinFET structure. A SiO_2 hard mask is used to protect the top of the SOI film during the long gate-etch process. **(b)** Key structural parameters are labelled. (Note that the oxide hard mask is not shown in this illustration for simplicity.)

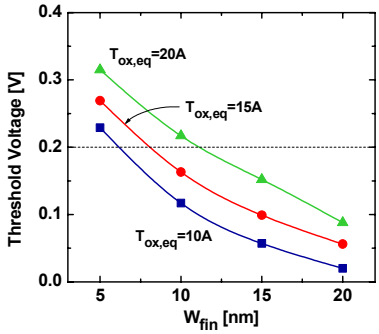

Figure 2: Dependence of FinFET threshold voltage on fin width and gate-oxide thickness for asymmetric (n+/p+ poly-Si) gates [9].

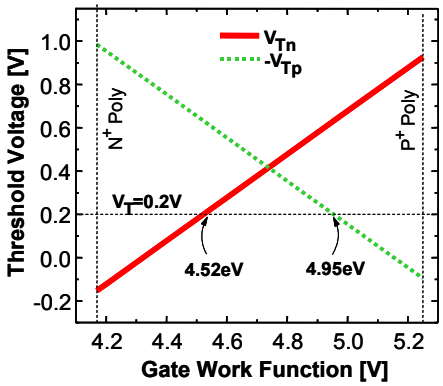

Figure 3: Dependence of n-channel threshold voltage (V_{Tn}) and p-channel threshold voltage (V_{Tp}) on gate work function, for fully-depleted SOI MOSFETs [11].

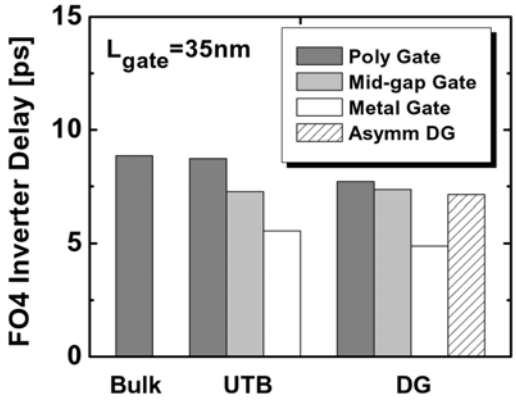

Figure 4: Comparison of loaded-inverter delay for thin-body SOI CMOS technologies against that for bulk-Si CMOS technology.

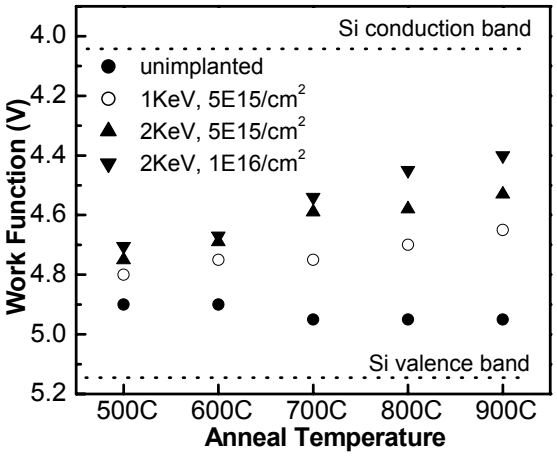

Figure 5: Dependence of Mo gate work function on post-N^+-implant annealing temperature and implant parameters [16]. All anneals were 15 minutes long, except for the 900°C anneal (15 seconds).

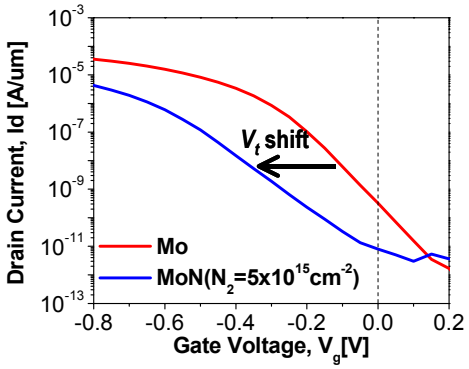

Figure 6: Measured transfer characteristics (I_D *vs.* V_G) of Mo-gated p-channel FinFETs (L_g=80nm, W_{fin}=10nm). Note that $|V_T|$=0.2V (defined at I_D=100nA/μm) is achieved without heavy body doping. Nitrogen implantation is effective for adjusting V_T.

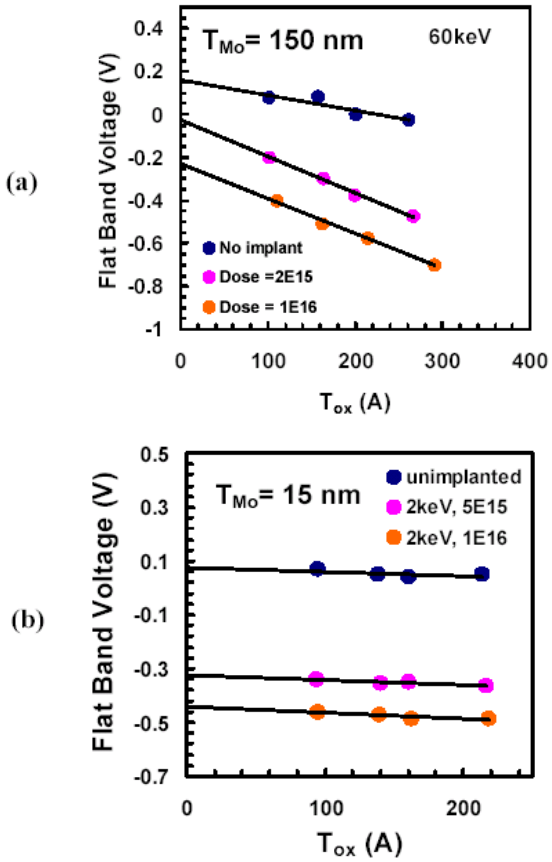

Figure 7: Flat-band voltage dependence on gate-SiO_2 thickness, for Mo-gated capacitors fabricated on bulk-Si substrates. ($V_{FB} = \Phi_M - \Phi_S - (Q_f/\varepsilon_{ox})\cdot T_{ox}$) For some devices, the Mo gate was implanted with $^{14}N^+$ to lower the gate work function. All devices were annealed at 900°C for 15s.

(a) Thick (150 nm) Mo gate devices; $^{14}N^+$ implant energy was 60 keV.

(b) Thin (15 nm) Mo gate devices; $^{14}N^+$ implant energy was 2 keV.

Degradation of the gate-dielectric interface (increased Q_f) is mitigated by reducing the $^{14}N^+$ implant straggle.

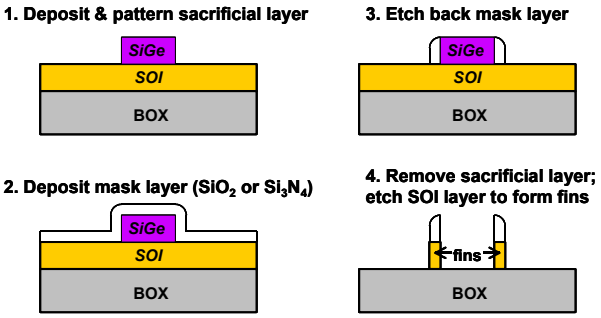

Figure 8: Sequence of schematic cross-sections illustrating the process for forming sub-lithographic fins using sidewall spacers as a hard mask.

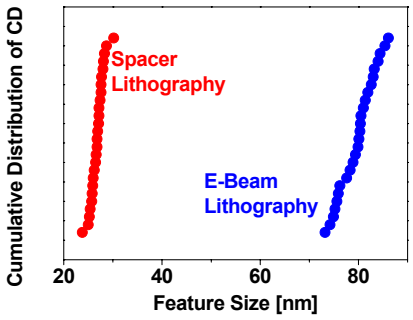

Figure 9: Comparison of CD uniformity achieved with a sidewall-spacer hard-mask process against that achieved with an e-beam lithography process [19].

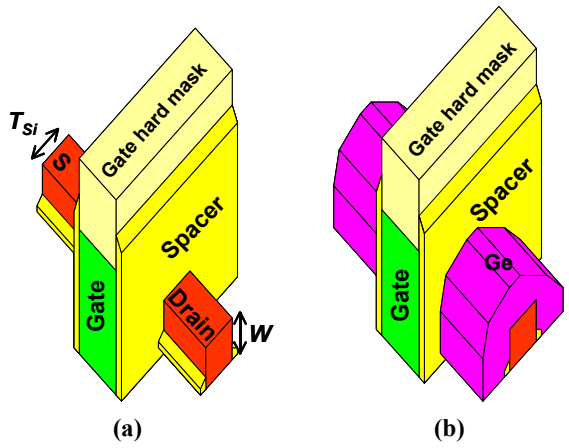

Figure 10: Illustration of raised-S/D fabrication process for a FinFET. **(a)** Structure after formation of gate-sidewall spacers. (The hardmask on top of the fin in the S/D contact regions is removed during the spacer etch.) **(b)** Structure after selective germanium deposition.

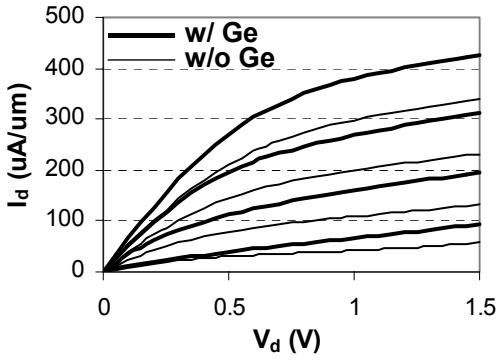

Figure 11: Measured output characteristics (I_D *vs.* V_D) of n-channel FinFETs with L_g=90nm and W_{fin}=70nm [22]. Significant improvement in drive current is achieved with the raised Ge-S/D structure.