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35nm CMOS FinFETs

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Abstract

We demonstrate for the first time high performance 35 nm CMOS FinFETs. Symmetrical NFET and PFET off-state leakage is realized with a simple technology. For 1 volt operation at a conservative 24 Å gate oxide thickness, the transistors give drive currents of 1240 μA/μm for NFET and 500 μA/μm for PFET at an off current of 200 nA/μm. Excellent hot carrier immunity is achieved. Device performance parameters exceed ITRS projections.

Introduction

The 2001 ITRS projected that below-10nm gate length will be launched before 2015 [1]. The most critical elements for continuing the current planar CMOS structure will be ultra thin gate dielectric (EOT should be less than 5Å), metal gate (to minimize gate depletion thickness), and ultra shallow junction (less than 10nm depth for reducing short channel effects). However, all of the three elements are "no known solution" so far. In contrast, with double-gate FinFET structure, an ultra shallow junction technology is not required to control short channel effects. Gate spacer can be shortened to reduce the parasitic series resistance and raise drive current. Furthermore, the FinFET reduces DIBL (Drain Induced Barrier Lowering). The requirements for thin gate dielectrics and metal gate can therefore be alleviated [2][3]. In this paper we demonstrate for the first time 35nm CMOSFETs using a simple in-situ doped N+ poly gate technology.

To explore the limit of accumulation-mode MOSFET (N+ gate on P-channel) is another goal of this study. For PMOSFET, N+ poly-Si gate has advantages of higher carrier mobility, no boron penetration from gate, and minimized depletion thickness of gate poly-Si. The short channel effects can be controlled in FinFET structure by simply thinning fin thickness.

Device Fabrication

The process flow used in this work is schematically illustrated in Fig.1, and the device structure is shown in Fig. 2. The starting material is (100) SOI wafers. The body thickness is thinned down by thermal oxidation and dilute HF dip. The fin height (channel width, represented by W_g) is up to 75nm, and with 9 nm cap oxide as shown in Fig. 3(a). Channel doping is performed to adjust NMOS V_t and PMOS V_t using masked ion implantation. Then, to relieve the etch damage, a sacrificial oxide is removed before gate oxidation. 24Å thermal oxide is grown and in-situ heavily doped N+ poly-silicon is deposited as shown in Fig. 3(b). After gate plasma etch, NFET source/drain extension implantation is performed and annealed. Composite spacer of silicon oxide and nitride is deposited and etched anisotropically with final thickness of ~30 nm. Heavily doped N+ and P+ junction are made with Phosphorous and Boron implantation. Thermal anneals above 1050°C are used for dopant activation. Cobalt-silicide is formed on the source/drain and gate to minimize the parasitic series resistance as shown in Fig. 3(c). After inter-layer-dielectric deposition, W is used for metal contact plugging and Cu is used for interconnection. Finally, alloying anneal (N_2/H_2, 400°C) is performed.

Results and Discussion

• 35nm CMOS FinFETs

Fig. 4 and Fig. 5 show the I_d-V_g and I_d-V_d characteristics of a 35 nm L_g and 28 nm fin thickness (T_{fin}) CMOS FinFETs. Drive currents of 1240 μA/μm for NFET, 500 μA/μm for PFET, and an off-state current of 200 nA/μm, are achieved for 1 V operation. By the more conservative definition of W_g being equal to two times of fin height, the drive current and off current will then be divided by two. Subthreshold swing is 78 and 96 mV/dec for NMOS and PMOS, respectively. As PMOS has higher swing compared to NMOS, a higher $V_{t,lin}$ for PMOS (-0.29 V) than for NMOS (0.13 V) is chosen for targeting the low off current. The transistor delay (CV/I) is 0.65 ps for NMOS and 1.7 ps for PMOS. Summary of transistor parameters in comparison with ITRS projection [1] and references of reported planar CMOS data [4~7] is shown in Table 1. Transistor performances (subthreshold swing and gate delay) of the FinFETs are comparable or exceed the references, and can be further significantly improved by the use of raised source/drain [8], thinner gate spacer [9], and replacing Cobalt-silicide with Nickel-silicide [6][7].

Fig. 6 exhibits the DC hot carrier reliability of the 35nm FinFETs. Both NMOS and PMOS have excellent hot carrier immunity, suggesting a possibility of further optimization of the LDD structure to improve drive current.

• 10nm CMOS FinFETs

Simulations are performed to study further scaling to 10nm gate length. Simulation results for FinFETs with 10Å gate oxide thickness are shown in Fig. 7. Three different gate material options are compared at the same off state leakage current of 200 nA/μm. The results confirm that N+ poly gate technology is unfavorable to PMOS current drive. Dual poly-gate technology and mid-gap gate technology can significantly improve PMOS performance and moderately improve NMOS performance.

Conclusion

CMOS double-gate FinFETs with 35 nm gate length are demonstrated. Fabricated NMOS and PMOS with symmetrical leakage meet ITRS projection in a CMOS technology. Accumulation-mode PMOS with a record 35 nm channel length is demonstrated. Simulations show that device performance can be improved with optional gate material. Excellent hot carrier lifetime is experimentally demonstrated for 35 nm CMOS FinFETs for the first time.

References

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 0-7803-7312-X/02/$17.00 ©2002 IEEE

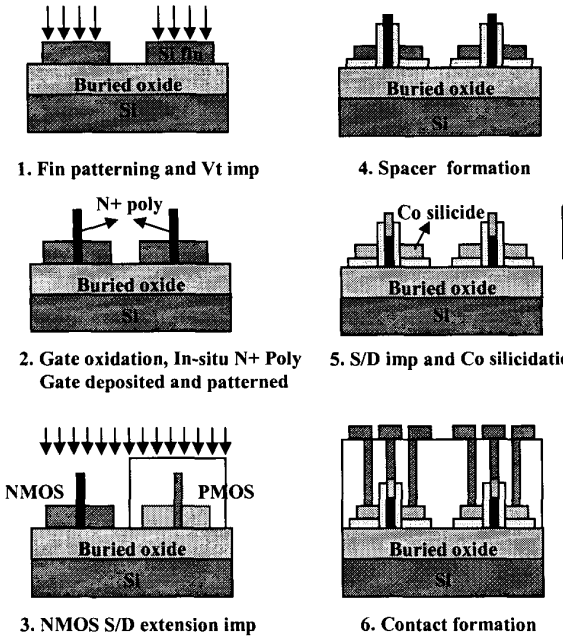

Fig. 1 Process flow chart of CMOS FinFETs.

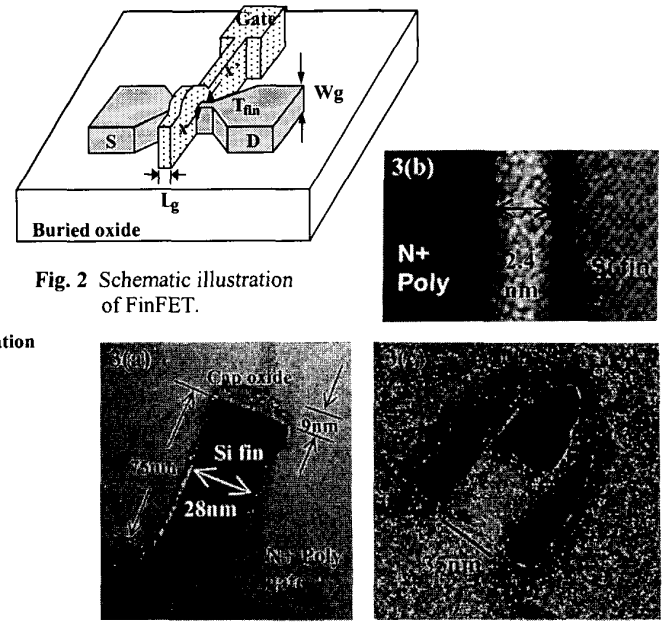

Fig. 2 Schematic illustration of FinFET.

Fig. 3 TEM cross-sectional views of (a) Si fin (x-x' direction in Fig.2), (b) gate oxide, and (c) Co-salicide gate.

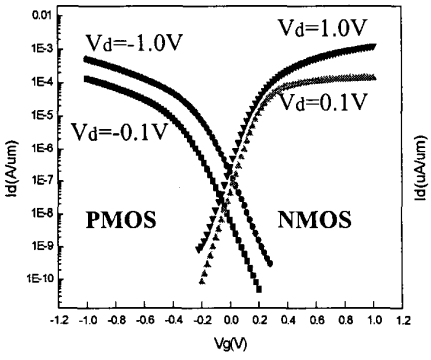

Fig. 4 Subthreshold Id-Vg characteristics of 35 nm Lg FinETs.

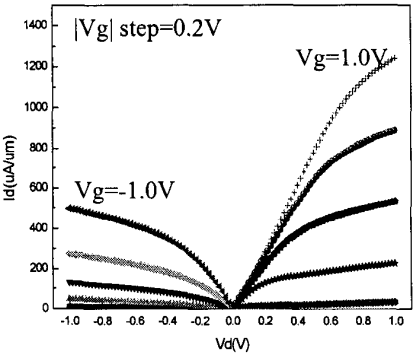

Fig. 5 Id-Vd characteristics of 35 nm Lg CMOS FinFETs.

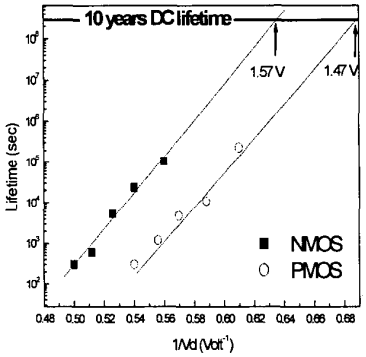

Fig. 6 Hot carrier lifetime evaluation of 35 nm Lg CMOS FinFETs.

	This work	ITRS [1]	Ref. [4]	Ref. [5]	Ref. [6]	Ref. [7]	Ref. [7]
Lgate [nm]	35	32 - 37	35	30	40	35	35
Vdd [V]	1	0.9 - 1.0	0.85	0.85	0.9	1	0.85
Tox (EOT) [Å]	24	8 - 14	7	8	9	10~12	10~12
Gate	in-situ N+	N+/P+	N+/P+	N+/P+	N+/P+	N+/P+	N+/P+
Salicide	Co	n.a.	Co	Ni	Ni	Ni	Ni
N, Idsat [μA/μm]	1240	900	580	514	657	871	676
N, Ioff [nA/μm]	200	100 - 300	50	100	100	141	100
P, Idsat [μA/μm]	500	n.a.	250	285	290	361	272
P, Ioff [nA/μm]	200	n.a.	90	100	100	80	100
N, Swing [mV/dec]	78	n.a.	95	100	n.a.	87	86
P, Swing [mV/dec]	96	n.a.	95	100	n.a.	98	92
N, CV/I [ps]	0.65	0.83-0.99	0.89	0.94	n.a.	n.a.	n.a.
P, CV/I [ps]	1.7	n.a.	1.8	1.7	n.a.	n.a.	n.a.

Table 1 Summary of transistor parameters. Comparison with ITRS [1] and references [4~7].

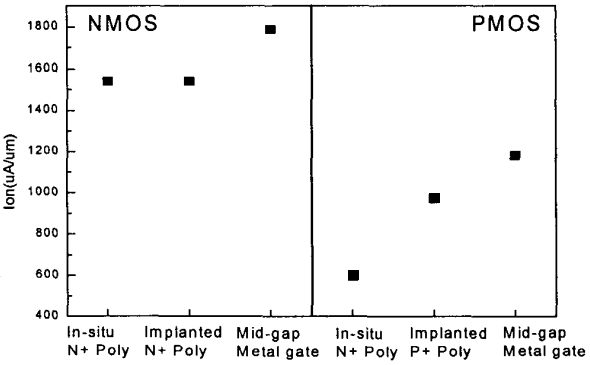

Fig. 7 Drive current simulations for 10 nm Lg CMOS FinFETs using 1.0 nm gate oxide thickness at I_{off} = 200 nA/μm and 0.8V operation, compared with three different gate material options: in-situ doped N+ poly gate, dual implant poly gate, and mid-gap metal gate.