Ultra-Thin Body PMOSFETs with Selectively Deposited Ge Source/Drain

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Abstract

Ultra-Thin Body (UTB) MOSFETs with body thickness down to 4nm and selectively deposited Ge raised source and drain (S/D) are demonstrated for the first time. Devices with gate length down to 30nm show excellent short-channel behavior. Mobility enhancement and threshold-voltage shift due to the quantum confinement of inversion charge by the ultra-thin body are investigated.

Introduction

The UTB MOSFET with raised S/D has been proposed to suppress short-channel effects and improve device performance [1]-[3]. Selective deposition of Ge would be an attractive technique for producing raised S/D because germane may provide an in-situ clean for the native oxide. Germanium S/D process only requires a low thermal budget (650℃, 20s RTA), which is attractive for compatibility with future high-K gate-dielectric materials. The process is fully CMOS compatible and much simpler and results in lower parasitic overlap capacitance than a previous UTB process [1].

Mobility enhancement has been predicted for n-channel UTB device when the UTB thickness is reduced to the inversion-layer thickness and the potential well presented by the UTB gives rise to subband splitting [4].

Quantum confinement also results in a smaller density of states so that more energy-band bending is required to attain a desired inversion-charge density as compared to a bulk-Si device. Thus, an increase in threshold voltage has been observed in thin-body devices [6][7].

Device Fabrication

The process flow used in this work is similar to that reported for UTB NMOSFETs reported in [2] except that TiN capped with poly-Si was used as the gate electrode to provide a mid-gap work-function in the present work. After sidewall spacer formation, 50nm Ge was selectively deposited onto the ultra-thin Si in the S/D areas by LPCVD to achieve the self-aligned raised S/D structure shown in Fig. 1 and Fig. 2. The selectively deposited Ge, as well as the 3nm ultra-thin body, 2.5nm gate oxide, and 3nm TiN metal gate can be seen in the TEM micrographs in Fig. 3. Adjacent to the spacers are two 60nm long oxide tails produced by incomplete spacer etch.

Results and Discussion

Fig. 4 shows the I_{ds}-V_{ds} characteristics of a 30nm L_g device with 4nm UTB. The 60nm-long oxide tails seen in Fig. 3 effectively produced 4nm thin and 60nm long S/D extension regions and resulted in high series resistance, which significantly degraded the drive current. These spacer tails can be easily eliminated with optimized spacer etch. Low leakage current (~10 pA/μm) is shown in Fig. 5. Fig. 6 shows excellent short-channel subthreshold swing even though the body-doping concentration (< 1.0×10^{15} cm^{-3}) is low. The threshold voltage is –0.60V, consistent with ultra-thin body with low body-doping concentration. Fig. 7 shows the hole-mobility dependence on UTB thickness. The mobility was extracted from the linear I_{ds}-V_{gs} data, from several devices at each body thickness. The maximum, minimum and average mobility values are shown in Fig. 7. The data indicate that mobility decreases with body thickness T_{Si} down to 5 nm, and then increases as the body thickness decreases further. This trend is similar to that expected for n-channel UTB FETs [4]. We believe that the enhancement in mobility for T_{Si} < 5nm, which is comparable to the inversion layer thickness, is caused by subband splitting in the valence band [5]. The subband energy of the 4-fold valleys is shifted up and occupancy of the 2-fold valleys increases, resulting in a decrease in mobility-effective-mass and an enhancement in mobility. Fig. 8 shows the dependence of threshold voltage on T_{Si}. If the V_t shifts were due to the dopant charge in the body, the NMOS and PMOS curves in Fig. 8 would have moved in the same direction. We conclude that the increase in $|V_t|$ for T_{Si} < 5 nm is due to the quantum confinement of the inversion charge.

Conclusion

Ultra-thin-body MOSFET with 30nm gate length is demonstrated. A selective Ge deposition process is developed to form self-aligned raised S/D regions with low thermal-budget and in-situ native oxide clean by germane. Enhancement of hole mobility is experimentally observed for body thickness below 5nm. The increase in threshold voltage with decreasing body thickness, due to the quantum confinement effect must be taken into account in the design of UTB devices, including the double-gate MOSFET.

Acknowledgement

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References

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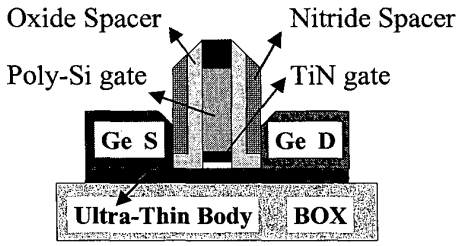

Fig. 1 Schematic cross-sectional view of UTB-FET with raised Ge S/D.

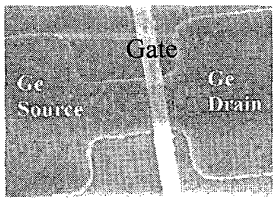

Fig. 2 SEM view of gate and raised Ge S/D.

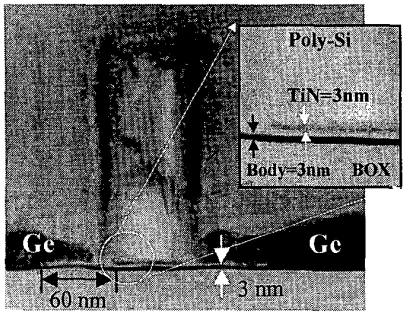

Fig. 3 TEM cross-sections of a UTBFET with 3 nm body thickness.

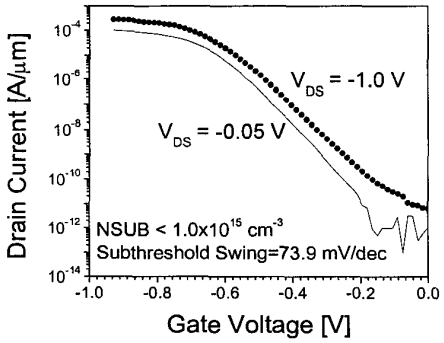

Fig. 4 Measured I_{ds}-V_{gs} characteristics of pMOSFET with L_g=30nm and T_{si}=4nm.

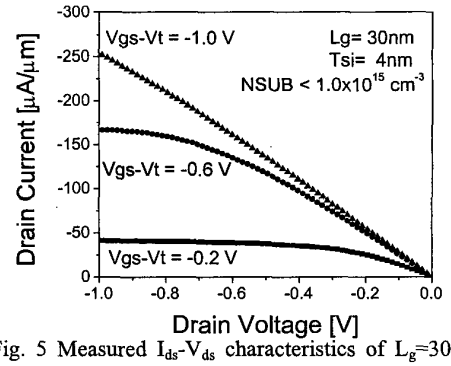

Fig. 5 Measured I_{ds}-V_{ds} characteristics of L_g=30nm and T_{Si}=4nm.

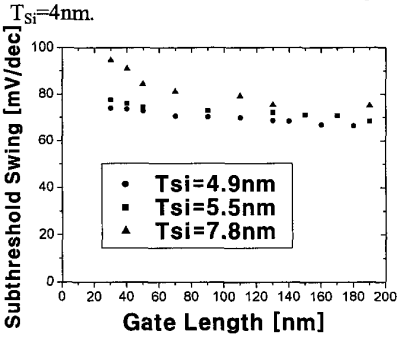

Fig. 6 Subthreshold swing vs. gate length.

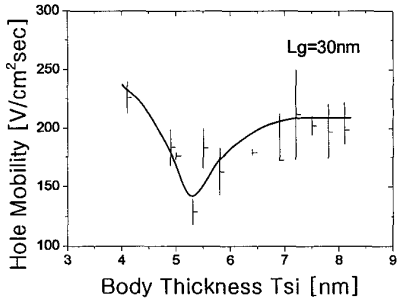

Fig. 7 Measured hole mobility vs. UTB thickness.

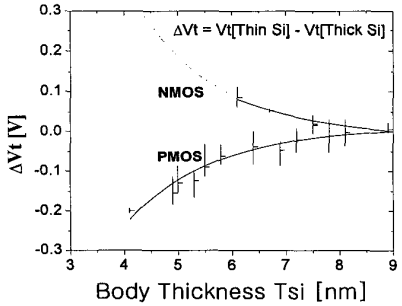

Fig. 8 V_t shift of NMOS and PMOS vs. UTB thickness.