Spacer FinFET : Nano-scale CMOS Technology for the Terabit Era

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Abstract

A spacer lithography process technology using a sacrificial layer and a CVD (Chemical Vapor Deposition) spacer layer has been developed, and is demonstrated to achieve sub-40nm structures with conventional dry etching. The minimum-sized features are defined not by photolithography but by the CVD film thickness. Therefore the spacer lithography technology yields CD (Critical Dimension) variations of minimum-sized features which are much smaller than achieved by optical or e-beam lithography. It also provides a doubling of device density for a given lithography pitch. This spacer lithography technology is used to pattern Si-fin structures for double-gate MOSFETs (FinFETs), and CMOS FinFET results are reported.

Introduction

Thin-body SOI devices are attractive for scaling CMOS into the nanoscale regime. One of the most promising structures is the FinFET with a double-gate that straddles a narrow Si-fin, which provides an ideal *60mV/dec* subthreshold swing and robustness against short-channel effects [1][2][3]. The thin-body minimizes sub-surface leakage paths between source and drain [4]. Nearly all the leakage current flows along the center of the fin where the electric potential is the least effectively controlled by the gate. Therefore, a thinner body allows for more aggressive gate-length scaling.

For the FinFET, short-channel effects can be suppressed by employing a body thickness (Si-fin width) which is approximately half of gate length L_g [2][5]. This is clearly impossible to accomplish with standard lithography technologies when L_g is at the limit of lithography. E-beam lithography has produced 15nm gates [6] and extreme-ultra-violet (EUV) lithography has generated sub-40nm lines [7]. But the throughput of e-beam lithography is too low and its uniformity is not yet satisfactory for deep sub-tenth micron gate length fabrication as shown in Fig. 1, and EUV lithography is not readily available yet.

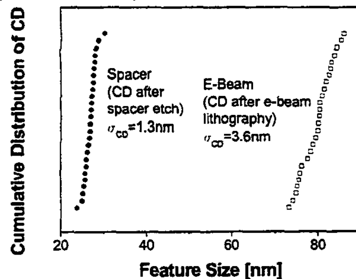


Fig. 1 CD variations of two lithography technologies. CD uniformity of the spacer technology is overwhelmingly better than e-beam lithography.

Uniformity is especially critical for the FinFET because variation in fin width (W_{fin}) can cause a change in the first quantized energy level of the inversion layer, giving rise to threshold voltage variation [8][9]. Also, if L_g/W_{fin} is smaller than 1.5, DIBL (Drain Induced Barrier Lowering), subthreshold swing, and leakage current increase significantly [2]. Higher Si-fin pitch than can be achieved with lithography is desirable, because multiple fins are needed to increase the effective channel width [10]. A high fin density is also required to obtain large transistor drive current with good layout-area efficiency.

Spacer lithography process technology is attractive for overcoming the limits of conventional lithography techniques in terms of pattern fidelity, CD variation, and pattern density. The spacer lithography technology described in this paper can produce extremely narrow and uniformly thick Si fins. One potential drawback of a conventional spacer technology is that it provides only one line width. But by combining a conventional masking process and the spacer process in a novel manner, we overcome this limitation. Si-fins down to 6.5nm are successfully formed, and 60nm gate length devices are successfully achieved.

Device Fabrication

Spacer lithography technology provides for a doubling of fin density, which doubles the drive current for a given lithography pitch, as shown in Fig. 2a and 2b.

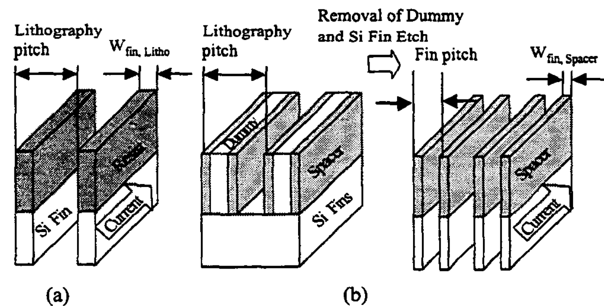


Fig. 2 Comparison of fin density achieved with (a) conventional lithography and (b) spacer lithography technology. The spacer lithography technology produces twice the fin density of a conventional lithography technology.

All masking processes used in this work were performed with i-line optical lithography, because its throughput is much better than e-beam lithography and the spacer lithography technology does not require very high resolution lithography. (100) SOI wafers were used as the starting material. The 100nm Si film was reduced to 50nm by thermal oxidation and 4nm thermal pad oxide was grown to relieve the stress between nitride hard mask and Si-fin. 50nm nitride was

deposited on the pad oxide serving as a hard mask to protect the Si-fin during the subsequent gate etch. 200nm sacrificial $Si_{0.4}Ge_{0.6}$ was deposited by LPCVD on the nitride hard mask and patterned (to support the spacers) with optical lithography and plasma etching. 10nm high temperature oxide (HTO) was then deposited by LPCVD over the patterned sacrificial $Si_{0.4}Ge_{0.6}$ layer. The thickness of HTO at the sidewalls of the sacrificial $Si_{0.4}Ge_{0.6}$ structures determines the final fin width. An extremely small fin width, beyond the lithographic limit, as well as very uniform fin width can therefore be obtained with this spacer lithography process. A subsequent anisotropic HTO spacer dry etch removed the HTO film on top of the sacrificial $Si_{0.4}Ge_{0.6}$ structure to generate an even number of spacers. Fig. 1 shows that the spacer technique provides very low CD variation compared to e-beam lithography with SAL601 resist.

Sacrificial $Si_{0.4}Ge_{0.6}$ was removed with (5:1:1) $H_2O:NH_4OH:H_2O_2$ at 75°C [11]. HTO, thermally grown oxide, nitride, and Si were not etched significantly in this solution. The resulting HTO spacer profile is shown in Fig. 3.

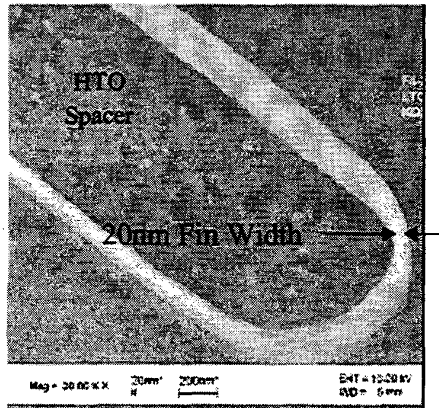


Fig. 3 SEM photograph of HTO spacer profile after removal of sacrificial $Si_{0.4}Ge_{0.6}$.

Optical lithography was used to define large S/D contact pads as shown in Fig. 4a. Therefore, the active Si was patterned with hard-mask HTO spacers for the fins and photo-resist for the S/D contact pad regions. One drawback of the spacer technique is that only one line width is provided. Variable fin widths were achieved by using photo-resist to define the fins as well as the S/D contact pads as shown in Fig. 4b. Spacers were used for the narrowest fins and the S/D contact pad mask was used for wide or variable-width fins.

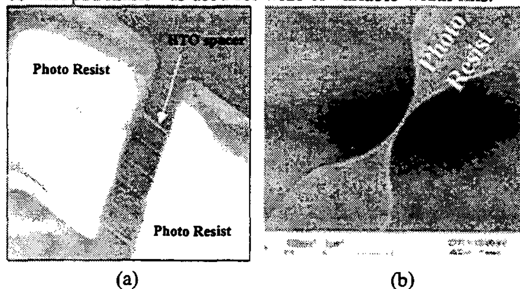


Fig. 4 Resist and HTO spacer profile for fin formation. (a) resist profile for S/D contact pad and HTO spacer profile for fin and (b) resist profile for varible-width fin. In terms of S/D extension resistance, (b) is better than (a).

An anisotropic Si-fin etch was used to define the Si-active area. Si fins as narrow as 6.5nm were obtained with the spacer lithography technology as shown in Fig. 5.

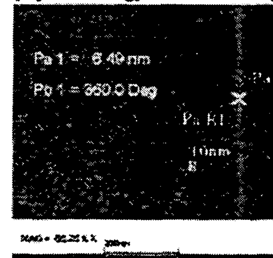


Fig. 5 6.5nm Si-fin profile after fin formation

A sacrificial oxidation step was used to remove the etch damage. 10nm of thermal oxide was grown in 12min @ 900°C in O_2. The sacrificial oxide was removed with diluted HF. Some part of buried oxide is etched and an undercut profile is produced as shown in Fig. 6.

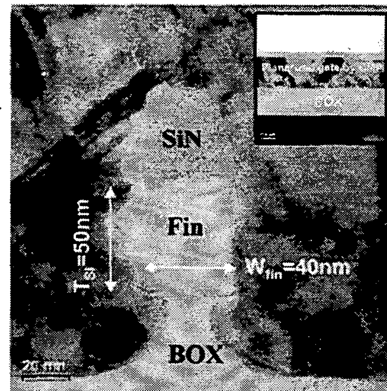
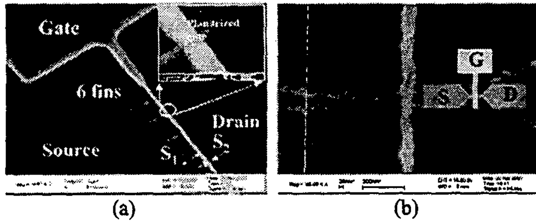


Fig. 6 TEM photographs of 40nm wide Si-fin and planarized gate profile after CMP (inset).

The gate oxide was grown at 750°C for 12min. $Si_{0.6}Ge_{0.4}$ deposited by LPCVD was chosen as the gate material. Planarized gate surface by CMP produced a large depth of focus (DOF) margin and wide etching window so that poly-SiGe stringers or residues were removed completely along the fin. 100nm gate hard mask oxide by LPCVD was deposited and phosphorus implantation was followed for gate doping. The gate was patterned over the fin using i-line lithography with a subsequent ashing-trimming technique [12] and etching processes as shown in Fig. 7a and 7b. 20nm spacer nitride and 10nm spacer oxide were deposited and double layer spacers were made after spacer etching. Masked S/D implantation and RTA (900°C, 1min) to make CMOS were followed. Metalization or silicide process was not used in this work and 400°C H_2 annealing was applied.



(a) (b)

Fig. 7 SEM photographs of (a) gate over 6 fins defined by spacer lithography and (b) gate over single fin defined by conventional lithography.

Spacer FinFETs Performances

Fig. 8 shows that gate current is reduced as a fin width decreases because of a reduction in the surface electric field in thin-body SOI [13].

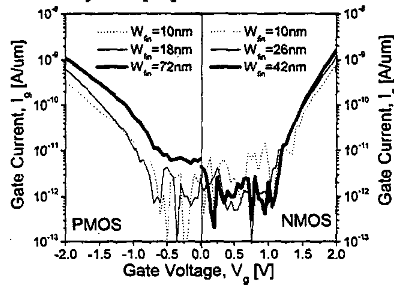


Fig. 8 Measured gate current vs. gate voltage. Narrower fin (thinner body) shows lower gate current.

Fig. 10 and Fig. 11 show CMOS subthreshold and drive current characteristics for 6-fin transistors defined using spacer lithography. All currents are normalized with 2^*T_{Si} (fin height in Fig.6) per fin, which is a conservative definition of the channel width in the double-gate. Fig. 12 and Fig. 13 show I-V characteristics of single-fin devices defined by conventional lithography. The relatively low NMOS drive current is due to a degraded electron mobility caused by Si-fin sidewall roughness generated by the dry etch process [14]. This degradation by surface roughness is more severe in NMOS than in PMOS because the inversion charge centroid of electrons is closer to the gate-oxide interface than that of holes as shown in Fig. 9. Relatively low drive current in the multi-fin devices caused by higher S/D extension resistance as shown in Fig. 4.

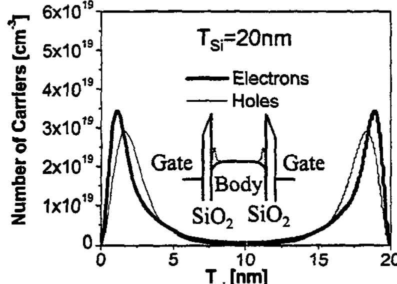


Fig. 9 Inversion charge centroid of electrons and holes at V_g-V_t=0.7V. This numerical simulation was performed with Shred [15].

Fig. 14 shows that drive current is strongly affected by extension resistance. Specific test structures were used to investigate the drive-current dependence on the series resistance, from the gap (S_2) between gate edge and S/D pad edge as shown in Fig. 7a. Fig. 15 shows that fin resistance is proportional to extension length and extracted doping concentration of fin is 1.2×10^{20} cm^{-3}. The gate is intentionally misaligned in the layout to produce different misalignment offsets between gate and S/D pad as shown in Fig. 7a. Fig. 16 shows V_t roll off characteristics and Fig. 17 shows subthreshold swing and drain induced barrier lowering (DIBL) dependence on gate length, respectively. Short-channel effects of PMOS are more than those of NMOS as shown in Fig. 10, 12, 16, and 17 because boron diffusivity in PMOS S/D is larger than phosphorus diffusivity in NMOS S/D for the same RTA condition.

Conclusion

A spacer lithography technology is developed for defining narrow Si fins for FinFETs. A 6.5nm wide Si fin was successfully defined, which is the smallest feature ever reported for a Si structure. This technology provides minimum feature size beyond the lithographic limit, better CD uniformity, and twice the device density. Sub-60nm FinFETs are demonstrated and show excellent short-channel behavior due to the double gate structure with thin body SOI.

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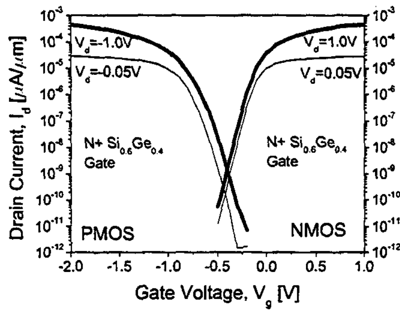

Fig. 10 Subthreshold I_d-V_g characteristics for L_g=60nm and W_{fin}=40nm, and T_{ox}=2.5nm (6 fins by spacer lithography)

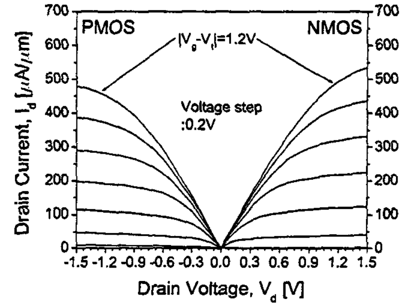

Fig. 11 I_d-V_d characteristics for L_g=60nm, W_{fin}=40nm, and T_{ox}=2.5nm (6 fins by spacer lithography)

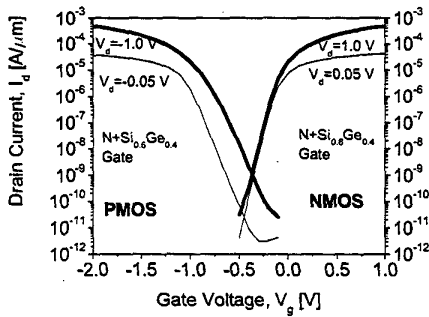

Fig. 12 Subthreshold I_d-V_g characteristics for L_g=60nm and W_{fin}=40nm, and T_{ox}=2.5nm (single fin by conventional lithography).

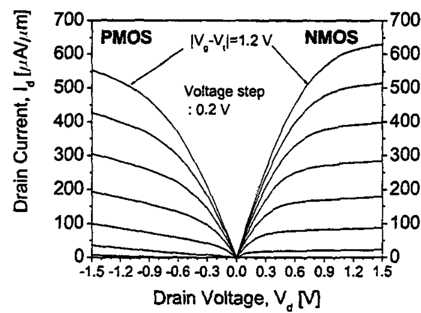

Fig. 13 I_d-V_d characteristics for L_g=60nm and W_{fin}=40nm, and T_{ox}=2.5nm (single fin by conventional lithography).

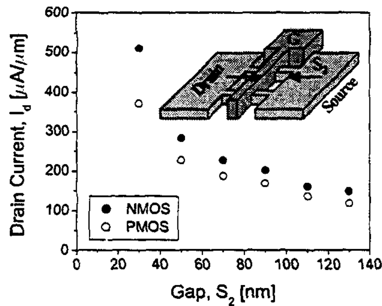

Fig. 14 Drive current dependence on extension length between gate edge and source pad.

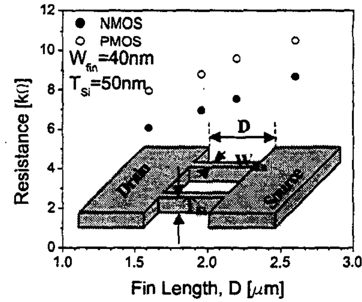

Fig. 15 Fin resistance dependence on the extension length, D.

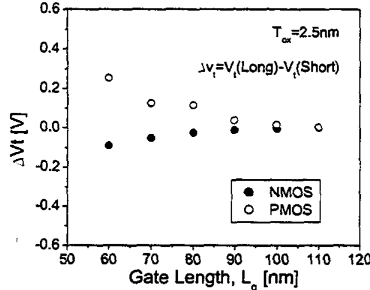

Fig. 16 Threshold roll off characteristics for CMOS.

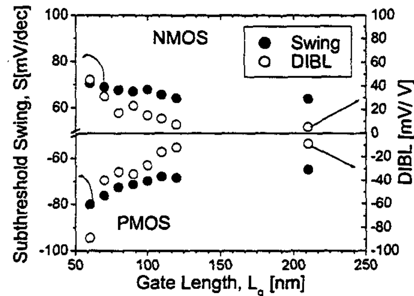

Fig. 17 Subthreshold swing and DIBL