Quasi-Planar NMOS FinFETs with Sub-100nm Gate Lengths

Nick Lindert, Yang-Kyu Choi, Leland Chang, Erik Anderson*, Wenchin Lee**, Tsu-Jae King, Jeffrey Bokor, and Chenming Hu.
Department of Electrical Engineering and Computer Sciences,
University of California at Berkeley, CA 94709
* X-ray Optics, Lawrence Berkeley National Laboratory, Berkeley, CA
** Now with Logic Technology Development, Intel Corporation, Hillsboro, OR
Email: nlindert@eecs.berkeley.edu

Introduction

Double-gate MOSFETs alleviate short channel effects and allow for more aggressive device scaling. Simulations have shown that scaling double-gated devices can reach 10nm [1,2]. In the past, process complexity has prevented serious development of a scalable double-gate device. In 1998, Hisamoto et al introduced a FinFET process that provided a method to fabricate devices with promising performance and scalability [3]. Using a single poly layer across a silicon fin to form both gates in the double-gate structure, the FinFET benefits from having equally-sized, self-aligned gates.

PMOS FinFETs were subsequently fabricated and showed excellent I_{on} and I_{off} [4]. Both reports used a similar process flow. In this work, we have revamped the FinFET process flow to make it simpler. This improved process flow still has the self-aligned double-gate advantage without suffering from extra gate-to-drain overlap capacitance.

Device Fabrication

The simplified FinFET device is illustrated in Figures 1 & 2. SOI wafers were thermally oxidized to provide 50nm silicon films with a 50nm hard mask oxide. Phosphorous implants were used to provide n-type channel doping in the range of $1e15cm^{-3}$ to $1e18cm^{-3}$.

The gate stack included a 500A oxide hard mask on top of 2400A in-situ boron-doped $Si_{0.5}Ge_{0.5}$ on 18A SiO_2 gate oxide. Si_xGe_{1-x} was used to engineer V_t [2]. E-beam lithography was used to define the critical fin and gate dimensions down to 50nm. Figure 3 shows a top view SEM of a 50nm gate across a 50nm fin prior to spacer formation. The gate-drain misalignment tolerance for this run was 100nm but tighter alignment can be achieved with improved e-beam stepping software.

After a spacer of 375A nitride on 100A oxide was formed, arsenic was implanted to form the source and drain. A 15 hour 600C anneal was used to recrystallize any portion of the silicon fin amorphized by the heavy As implant. This was followed by a short 900C activation anneal and a 450C forming gas anneal.

Results

Device results for a 90nm gate across a 80nm fin are shown in Figures 4 & 5. The width of a FinFET device is 2*(fin height)*(number of fins). All devices in this work use a single fin so W is 100nm. Larger W devices are possible with multiple fins [3,4]. In Figure 4, using V_g-V_t=1V and V_d=1V we evaluate I_{dsat} ~ 375uA/um. An alternative, more aggressive definition of W as simply the fin height would effectively double the reported current to 750uA/um. Despite using n-type channel doping in the range of $1e15cm^{-3}$ to $1e18cm^{-3}$, the NMOS V_t remained ~1V, higher than expected for a p-type $Si_{0.5}Ge_{0.5}$ gate. This insensitivity to channel doping shows the importance of the gate workfunction for scaling double-gate devices.

FinFET turnoff characteristics depend heavily on the fin width as shown in Figure 6. This data suggests that L_{gate}, in this case study, can be scaled down to 1.3 times W_{fin} without suffering from excessive leakage current, even with n-type channel doping. The minimum W_{fin} fabricated for this work is 50nm so L_{min} ~ 65nm as shown in Figures 7 & 8. Such de-coupling of short channel effects and channel doping is critical for scaling MOSFETs down to 10nm.

Conclusion

A simplified FinFET process was developed and first NMOS results are shown. Data suggest that FinFET scaling is very promising. Improved current for future devices can be realized by lowering V_t with improved gate workfunction engineering and with thinner T_{ox}. Further improvements can be made by using a raised S/D [5-6] or silicided S/D.

Acknowledgement

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References

[1] L. Chang et al., Nanoelectronics Workshop 2000, p351.
[2] L. Chang et al., IEDM 2000, p719.
[3] D. Hisamoto et al., IEDM 1998, p1032.
[4] X. Huang et al., IEDM 1999, p67.
[5] Y.-K. Choi et al., IEDM 1999, p919.
[6] Y.-K. Choi et al., DRC 2000, p23.

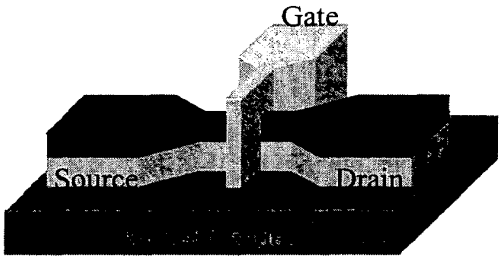

Fig. 1. 3D view of FinFET using simplified process flow.

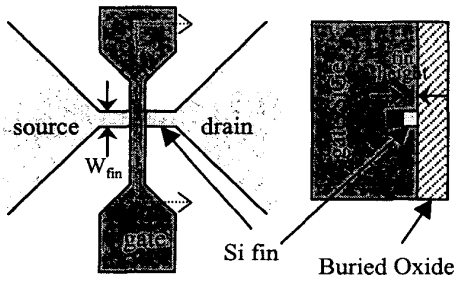

Fig. 2. FinFET layout and cross sectional view. Because the gate modulates the current on both sides of the fin, the transistor W is considered to be twice the fin height.

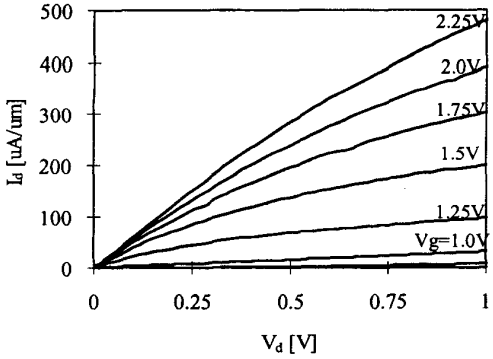

Fig. 4. I_d-V_d curves for a 90nm gate over a 80nm fin. V_t~0.9V so $I_d(V_g\text{-}V_t\text{=}1V; V_d\text{=}1V)$ ~ 375uA/um or 750uA/um if W is defined as one fin height.

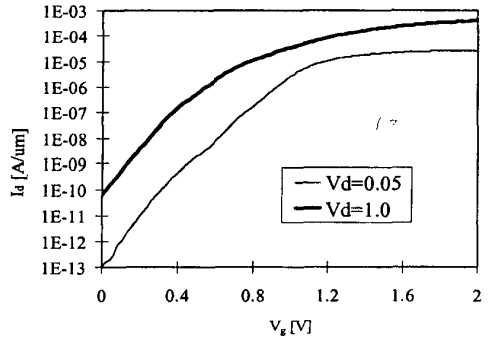

Fig. 5. I_d-V_g curves for a 90nm long gate over a 80nm fin.

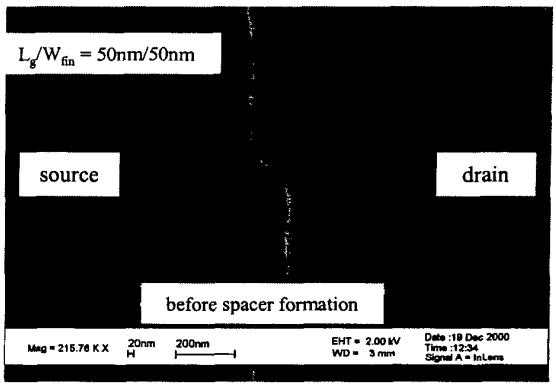

Fig. 3. Top view SEM after gate definition for 50nm gate and 50nm fin.

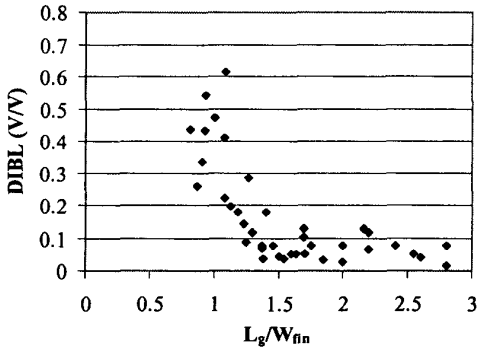

Fig. 6. DIBL is the shift between Vd=50mV and Vd=1V evaluated at 1e-8A/um. The gate should be at least 1.3 times the width of the fin to provide adequate turnoff.

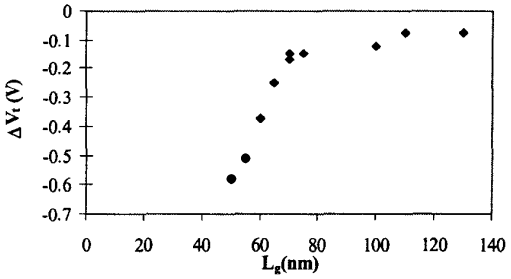

Fig. 7. V_t rolloff for W_{fin} = 50nm. L_{min} ~ 65nm

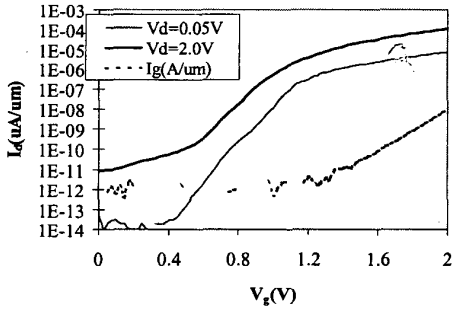

Fig. 8. I_d-V_g curves for L=65nm, W_{fin} = 50nm