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Quasi-Planar FinFETs with Selectively Grown Germanium Raised Source/Drain

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Introduction

Double-gate MOSFETs are attractive because they can be scaled to the shortest gate length for a given gate oxide thickness [1]. Recent studies suggest that double gate devices can meet performance requirements down to 10nm gate length [2]. The FinFET was introduced in [3] and is a promising double-gate structure. In [4], a simplified, quasi-planar version of the FinFET exhibiting excellent performance was presented.

Short channel effects can be suppressed in the FinFET provided that the gate length is at least 1.4 times the fin thickness [4,5]. The source/drain (S/D) thin fin extension regions are highly resistive so it is essential to minimize the length of the S/D thin fin extensions. In this work, we combine the simplicity of the new FinFET process flow with a selective Ge growth technique to present the first raised S/D quasi-planar FinFET devices.

Device Fabrication

The quasi-planar FinFET device is illustrated in Figures 1 & 2. SOI wafers are thermally oxidized to provide 50nm silicon films with a 50nm hard mask oxide. E-beam lithography is used to form silicon fins as narrow as 35nm and then the gate stack is formed, comprised of a 50nm oxide hard mask on top of 240nm in-situ boron-doped poly-$Si_{0.5}Ge_{0.5}$ on 1.8nm SiO_2 gate oxide. A top-view SEM image of a multifin device just after gate patterning is shown in Figure 3.

After a double-layer spacer of 37.5nm nitride on 10nm oxide is formed, arsenic and phosphorus are implanted to form the self-aligned S/D. A 15 hour 600°C anneal is used to recrystallize any portion of the silicon fin amorphized by the heavy As implant. This is followed by a short 900°C activation anneal and a 450°C forming gas anneal.

After completely removing the oxide over the S/D regions, 70nm of Ge is selectively grown by LPCVD to provide the desired raised S/D. A TEM image of Ge selectively grown on a Si test wafer is shown in Figure 4. A similar technique has been used for ultra-thin body SOI MOSFETs [6]. A top-view SEM image of a FinFET (with poor alignment) after selective Ge growth is shown in Figure 5. Ge growth can clearly be seen. The Ge thickness was limited to 70nm to avoid bridging between the gate and the S/D. The Ge growth is followed by a phosphorus implant, 750°C activation anneal, and a 400°C forming gas anneal. No silicide or metal was used in the devices reported here.

Results

Measured I-V characteristics for a 90nm FinFET with 70nm fin width are shown in Figure 6. An Idsat improvement of up to 28% results from the raised S/D processing. The absence of excessive gate current indicates that bridging between the gate and S/D did not occur.

Because the gate is not self-aligned to the wide S/D regions in the quasi-planar FinFET, S/D resistance can be asymmetric, particularly noticeable when the original fin width is small. The I-V characteristics shown in Figure 7 are for a raised S/D quasi-planar FinFET with alignment similar to the device shown in Figure 5. Reversing the source and drain changes Idsat by only 3%. Thus, even with poor alignment, the impact of asymmetry on the performance of a raised S/D quasi-planar FinFET is minimal.

Conclusion

High performance NMOS quasi-planar raised S/D FinFETs are presented. Current for these double-gate devices is enhanced by as much as 28% with a Ge raised S/D process. Worst case misalignment is shown to produce only a minimal 3% degradation in drive current. Siliciding the S/D fins could further reduce this penalty.

Acknowledgement

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References

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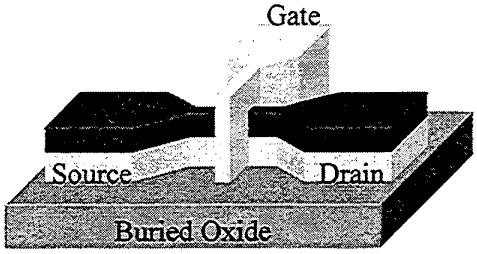

Fig. 1. 3D view of quasi-planar FinFET.

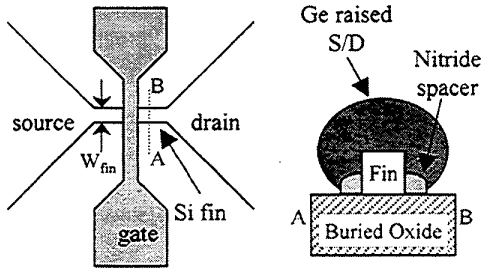

Fig. 2. FinFET layout and cross sectional view. The cross section shows the fin after selective growth of ~70nm raised S/D.

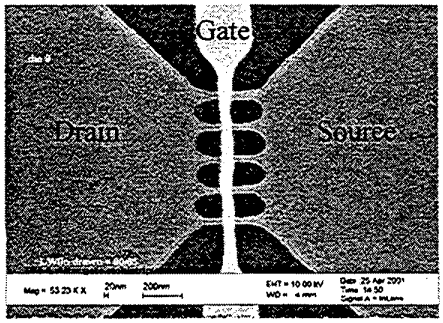

Fig. 3. SEM top view of multifin device prior to spacer formation and selective Ge growth. L_g/W_{fin} ~ 50/35nm.

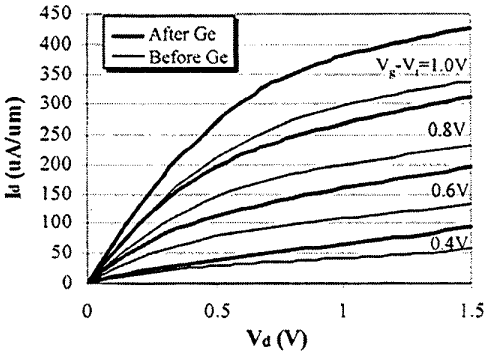

Fig. 6. I_d-V_d for L_g/W_{fin} = 90/70nm single fin FinFET. A 28% increase in I_{dsat} results from Ge raised S/D. W = 2*(fin height) = 100nm.

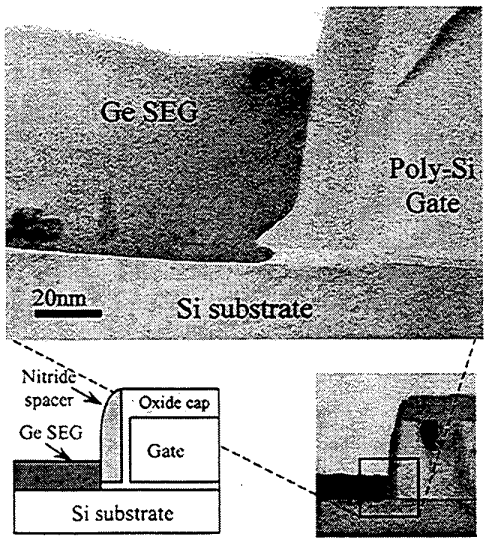

Fig. 4. TEM cross-sectional image of selectively grown Ge on a bulk-Si test wafer. The deposition is perfectly selective to both nitride and oxide.

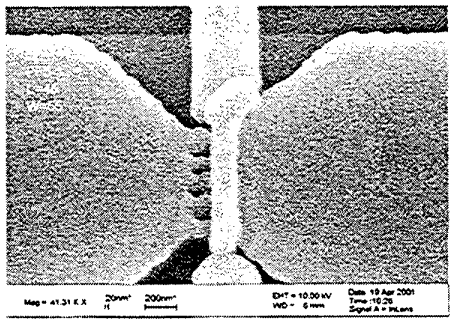

Fig. 5. SEM top view of a sub-50nm gate multifin device after selective Ge growth. Ge was selectively grown on both the gate and the S/D without bridging.

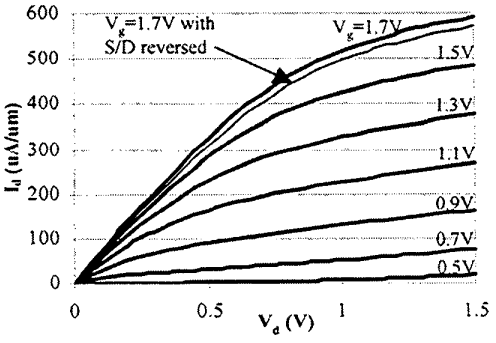

Fig. 7. I_d-V_d for FinFET with poor misalignment. The thinner line for V_g=1.7V shows the effect of reversing the source and drain connections.