Patterning Sub-30-nm MOSFET Gate with I-Line Lithography

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Abstract—We have investigated two process techniques: resist ashing and oxide hard mask trimming. A combination of ashing and trimming produces sub-30-nm MOSFET gate. These techniques require neither specific equipment nor materials. These can be used to fabricate experimental devices with line width beyond the limit of optical lithography or high-throughput e-beam lithography. They provide 25-nm gate pattern with x-line lithography and sub-20-nm pattern with e-beam lithography. A 40-nm gate channel length nMOSFET is demonstrated.

I. INTRODUCTION

Currently, MOSFET gate length for advanced research is below 50 nm. Making such a small feature is not an easy task, in general. Although e-beam lithography employing some positive resists such as PMMA has high resolution, its throughput is too low even for research.

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We will discuss two techniques that provide sub-30-nm line width without using any special equipment or materials. The first technique is resist ashing. This technique was developed for making submicron devices from g-line lithography about ten years ago [1]. Since then, it has been rather widely used to produce smaller features than the resolution limit of optical lithography [2]–[4]. The second technique is an oxide hard mask trimming. Oxide hard mask trimming is relatively straightforward, but we have found no reports that describe it, let alone report on its use in the sub-30-nm regime. A combination of these two techniques makes it possible to fabricate 25 nm line width using i-line lithography.

II. EXPERIMENTS AND RESULTS

A. Ashing of i-Line Resist

Sample wafers were exposed with an i-line stepper. The thickness of the positive i-line resist was 1.1 μm and baked at 90 °C for 1 min before exposure and 120 °C for 1 min after exposure, respectively. The resist patterns after a development were ashed in an oxygen-plasma asher, Technics PE II. Oxygen pressure was 260 mTorr with a flow rate of 51.1 sccm.

The ashing rate of the i-line resist without hard baking (120 °C) is shown in Fig. 1. The vertical ashing rate is the rate of reduction of the resist thickness, while the horizontal ashing rate is the rate of reduction of the line width. Both ashing rates change linearly with the ashing power and are independent of the initial line width.

The ratio of the horizontal ashing rate to the vertical ashing rate is about 1.2:1, which produces isotropic profile. Ashing does not change the edge roughness of the resist as shown in Fig. 2(a). The smoothness of the initial lines is very important for good ashing results. In the case of i-line lithography, line smoothness depends strongly on the mask quality.

The taper angle of the narrow resist profile at the top corner increases slightly after ashing. The top of the resist may be rounded in the end. This can happen earlier in narrow lines than in wide patterns. Even if the top of the resist is rounded off, etching does not present a problem as long as the resist is thick enough.

B. Ashing e-Beam Resist

Two chemically amplified resists, SNR-2000 and SAL601, were evaluated. Ashing of the e-beam resists was done in the same asher, Technics PE II.

In the case of e-beam resist patterns, only a small amount of ashing compared to i-line patterns is needed because the initial line width is 100 nm or less. We fixed the ashing power at 5 W, which was the lowest power to sustain stable plasma. The ashing rates of the e-beam resists are 22–30 nm/min at 5 W power. For SAL and SNR, the ashing rates were almost the same.

One interesting phenomenon is resist hardening caused by SEM. Since SAL and SNR are negative resists, they are hardened by the exposure to e-beam (energy is less than 1 KeV) during SEM. After SEM, ashing rate of the resist patterns exposed to the e-beam decreased to two-thirds of those not exposed.

In Fig. 3(a), the SEM picture of a 17-nm ashed SNR-2000 resist line is shown. This line was originally 80-nm wide after e-beam lithography.

C. Oxide Hard Mask Trimming

The concept of oxide hard mask trimming is similar to the resist ashing. After the ashing-down of the gate resist patterns, an oxide hard mask pattern is anisotropically etched. A Lam research model
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9400 TCP etcher is used for the anisotropic etching. The etching condition is 90 sccm CHF$_3$ and 200 sccm Ar plasma, 20 mTorr, 200 W RF top power, and 40 W RF bottom power. For 120 nm of high temperature oxide (HTO) etching and 20% overetching, 70 s is required.

The patterned oxide hard mask is etched to a desired smaller size in HF solution. In this case, the etching is isotropic as expected. Typical etch rate of HTO is about 30 nm/min in 25:1 HF in our experiments. After hard mask trimming, the gate polysilicon is etched quite easily without any photoresist. There were no polymer films left after the gate polysilicon etching. Hard mask trimming is especially useful when the resist thickness is too thin to be used for the resist ashing.

A 500-nm i-line resist was ashed down to 80 nm and transferred into the oxide hard mask with anisotropic etch. The oxide hard mask was then trimmed to 30 nm isotropically from 80 nm with (25:1) HF solution, as shown in Fig. 2(b). Fig. 2(c) shows the top view of a polysilicon gate, which was etched with the trimmed oxide hard mask serving as the etching mask. The polysilicon etching is performed with Lam 9400 TCP etcher. The etching condition is 50 sccm Cl$_2$ and 150 sccm HBr, a pressure of 15 mTorr, 200 W RF top power, and 120 W RF bottom power for main etching. 200 sccm HBr, 5 sccm O$_2$, 35 mTorr, 250 W RF top power, and 150 W RF bottom power is used for 100% overetching. A 7 s main etching and 60 s overetching is required to etch 180 nm polysilicon.

Fig. 3(b) shows an isotropically trimmed oxide hard mask pattern, which was initially 80 nm by e-beam lithography. Fig. 3(c) illustrates a 20-nm gate polysilicon profile of a SOI MOSFET, which was patterned with the trimmed oxide hard mask. Metal gate has been proposed to suppress the gate depletion and to adjust threshold voltage for midgap engineering. Oxide hard mask trimming is also compatible with metal gate.

D. Device Performance

N-channel MOSFET is fabricated on the ultrathin body (20 nm) SOI wafer to suppress the short-channel effect [5], [6]. A 40-nm gate length nMOSFET is demonstrated. Fig. 4(a) shows $I_{ds}$-$V_{gs}$ characteristics and $V_{th}$-$V_{ds}$ characteristics. DIBL is suppressed, as shown in Fig. 4(b), and the subthreshold swing is 87 mV/dec.

III. CONCLUSION

For optical and e-beam lithography, resist ashing is a convenient technique to overcome the lithographic limit of minimum feature size. An oxide hard mask trimming is also a useful technique to obtain small features. A combination of these two techniques can produce very small features for research purposes. The 25-nm MOSFET gate length is defined with i-line technology and sub-20-nm gate length is defined with e-beam lithography. A 40-nm gate channel length nMOSFET is demonstrated.

REFERENCES

Gate-Induced Drain Leakage Current Enhanced by Plasma Charging Damage

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Abstract—Correlation between gate-induced drain leakage current (GIDL) current $I_{GIDL}$ and plasma charging damage is investigated for the p-MOSFETs. $I_{GIDL}$ and maximum charge pumping current show the same trend as a function of antenna area ratio (AAR) and cell location. Enhancement of $I_{GIDL}$ is mainly attributed to the increase of Si/SiO$_2$ interface traps generated in the plasma processes and is not related to the small amount of trapped charge in the oxide.

Index Terms—CMOSFET, leakage current, plasma charging damage.

I. INTRODUCTION

Gate-induced drain leakage current (GIDL) [1] is a major source of off-state current. It is important to understand the causes of GIDL since it is essential to minimize the off-state current in the low-power integrated circuits. For a fresh MOSFET, GIDL is attributed to band-to-band tunneling process at Si/ SiO$_2$ interface due to the gate-induced high field at the deep-depleted gate-to-drain overlap region [1], [2]. There are also some works concerning the enhancement of GIDL as a symptom of MOS device degradation. Chen et al. [3] and Hori [4] observed that band-to-defect tunneling via the Si/ SiO$_2$ interface traps enhances GIDL in MOSFET. More recently, Wang et al. [5] and Lai et al. [6] developed an interface trap-assisted two-step tunneling model for increased GIDL after hot-carrier stress. On the other hand, Lo et al. [7] argued that both Si/ SiO$_2$ interface traps and oxide-trapped charge play important roles in the GIDL degradation.

Plasma-induced damage (PID) in gate oxide has been a major concern in the manufacture of deep submicrometer MOSFETs [8]–[10]. Plasma processes can introduce constant Fowler-Nordheim (FN) current stress, which results in gate oxide degradation or even breakdown [11], [12]. Gate oxide degradation by PID may cause variations of device parameters such as threshold voltage $V_{th}$, subthreshold swing $S_S$, transconductance $G_m$ [8], [10], etc. Both PID and GIDL have strong relations with the gate oxide degradation. However, there is no report of plasma charging effect on GIDL. It is not obvious whether PID will induce detectable change of GIDL, since PID is induced by area uniform current stress, while a very local region close to the drain mainly affects GIDL. This brief investigates the correlation between GIDL and PID in thin gate oxide MOSFETs.

II. EXPERIMENT

The devices used to evaluate the plasma charging damages were $20 \mu m/0.4 \mu m$ poly-silicon gate p-channel MOSFETs with 50 Å gate oxide. Different antenna structures were fabricated in metal 1 layer. An HP4156A parameter analyzer was used for device parameter extraction. Interface traps were measured using charge pumping technique [13], [14]. The gate pulses, supplied by an HP8112A pulse generator, have a fixed high level $V_h$ and varying base level $V_b$ with 50% duty cycle with a frequency of 200 kHz and a 50 ns rise/fall gradient. During the charge pumping measurement, the trapezoidal pulse is applied to the gate, the substrate is grounded, and the dc charge pumping current is measured from either drain junction or the substrate while the source junction is left floating [13]. This test configuration enables us to eliminate the contribution from the interface traps at the source junction and extract specific signal related to the interface traps for our interests concerning GIDL.

III. RESULTS AND DISCUSSION

Fig. 1 shows the subthreshold characteristics for $p^+/p$ MOSFETs with different antenna area ratio (AAR) in the same cell location. As can be seen, compared with the reference device (no antenna), there is a significant increase in GIDL current $I_{GIDL}$ in the devices with antenna structure. $I_{GIDL}$ magnitude increases with increasing AAR. In this briefly, all $I_{GIDL}$ are defined as drain current measured at the fixed condition of $V_g = 0$ V and $V_d = -3.3$ V. In Fig. 2(a), the $I_{GIDL}$ magnitudes of $p^+/p$ MOSFETs with different AAR are plotted as a function of cell location. The measurements were carried out on seven cells along a central line across the wafer. It can be seen that $I_{GIDL}$ changes regularly according to the distance between the device site and...