30nm ultra-thin-body SOI MOSFET with selectively deposited Ge raised S/D

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Abstract

MOSFETs with selectively deposited Ge raised S/D implemented in 8nm ultra-thin-body (UTB) SOI are demonstrated. The Ge is selectively deposited by LPCVD and annealed at a low temperature using RTA (650C, 20sec). Devices with gate length down to 30nm are obtained with 8nm UTB and show excellent short-channel behavior.

Introduction

Fully depleted Silicon-On-Insulator (SOI) technology has the advantages of lower junction capacitance and better subthreshold swing [1]. However, the conventional fully depleted SOI MOSFET is known to have worse short-channel effects than bulk MOSFETs and partially depleted SOI MOSFETs [2]. The ultra-thin-body (UTB) structure eliminates the leakage paths between source and drain [3] [4] and provide a more evolutionary alternative to the vertical or surround-gate MOSFET for deep-sub-tenth micron technology. It overcomes the dopant-number fluctuation or Vt fluctuation scaling limit as well. Thicker self-aligned source and drain (S/D) structures minimize parasitic series resistance to achieve excellent performance. Selective Ge deposition is a promising technique for making the thicker S/D and also has the benefit of a low thermal budget. It is much simpler and provides lower parasitic overlap capacitance than a resist and poly etch-back process [4]. Also it is fully CMOS compatible.

Device Fabrication

100nm thickness p-type ($<1.0\text{x}10^{15}$ cm^{-3}) SOI films (BOX=400nm) were reduced to 8nm by thermal oxidation. Isolation was achieved with a simple silicon etch as shown in Fig 1 a. The 2nm thin gate oxide was grown at 750 ^{o}C in 13min and annealed at 900 ^{o}C in 30min. N+ in-situ doped poly-Si was deposited and hard mask oxide was deposited to shield the gate poly-silicon during Ge deposition.

Gates down to to 30nm were patterned as shown in Fig. 2 a and double spacers composed of an inner oxide and an outer nitride were formed as shown in Fig. 1 b. The purpose of the double spacers is to protect the thin- body active area during the spacer etch, which consisted of a dry etch followed by a wet etch using HF.

160nm Ge was selectively deposited on the thin-body Si active areas to make a self-aligned raised S/D as shown in Fig. 1 c and Fig. 2 b. No Ge was deposited on the spacer nitride and hard mask oxide because of the extremely high selectivity. The selective Ge deposition was performed using conventional LPCVD. The process conditions were 350 ^{o}C, 300mTorr, and 200sccm GeH_4. High dosage phosphor implantation followed. A 650 ^{o}C, 20sec RTA was used for activation and device fabrication was completed with a 400 ^{o}C forming gas anneal.

MOSFET Characteristics

Fig. 3 shows the Ids-Vds characteristics for a 30nm gate length device (W=10um). The saturation current is low due to high series resistance. The measured series resistance is 1kΩ and ΔL is 10nm. The RTA conditions for this novel process have not yet been optimized.

Fig. 4 shows Ids-Vgs characteristics for a 30nm gate length device. 30nm NMOS with 8nm UTB shows excellent short-channel behavior. Subthreshold swing is 73mV/dec. The threshold voltage is very low (-0.20V@100nA/um and –0.11V for linear extrapolation) This is caused by low body doping ($<1.0\text{x}10^{15}$ cm^{-3}). Vt can be adjusted using gate work function engineering [4] [5].

Fig. 5 shows Vt roll-off characteristics, which is dependent on body thickness. Fig. 6 shows subthreshold swing as a function of body thickness. Subthreshold swing is less sensitive to channel length with a thinner body. Short-channel effects are more suppressed with the thinner body, as expected. If the gate length (Lg) is larger than twice the body thickness (Tsi), the device is successfully scaled down.

Conclusion

A 30nm gate length with 8nm thin body nMOSFET is demonstrated. A selective Ge deposition process is used to form self-aligned raised S/D. This novel process provides low thermal budget and CMOS compatibility and with further optimization of post-deposition annealing conditions, should result in low parasitic resistance and capacitance for excellent performance.

Acknowledgement

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References

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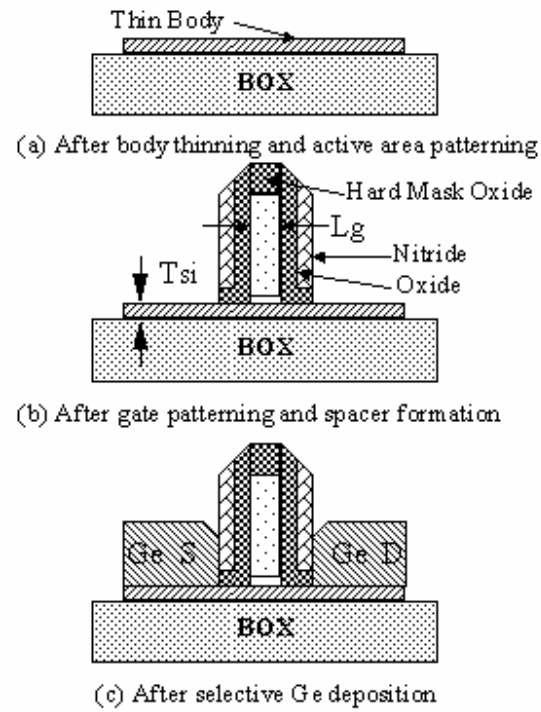

Fig. 1 Process flow of selective Ge S/D UTB SOI device.

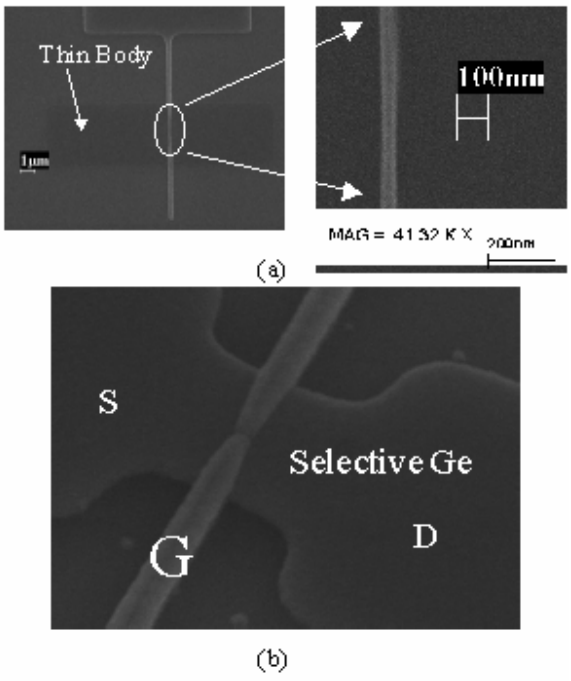

Fig. 2 SEM pictures of (a) 30nm gate length and (b) selectively deposited Ge raised S/D.

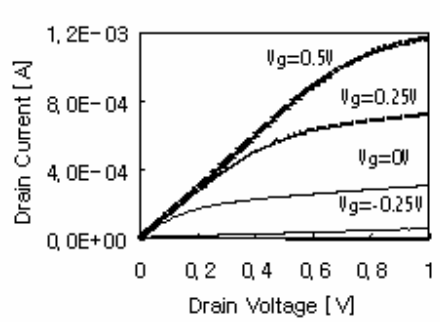

Fig. 3 UTB SOI nMOSFET Ids-Vds characteristics of 30nm gate length and 8nm Tsi (W=10um).

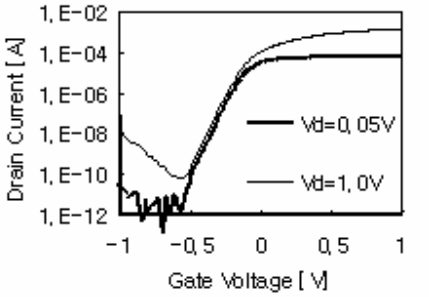

Fig. 4 UTB SOI nMOSFET Ids-Vgs characteristics of 30nm gate length and 8nm Tsi (W=10um).

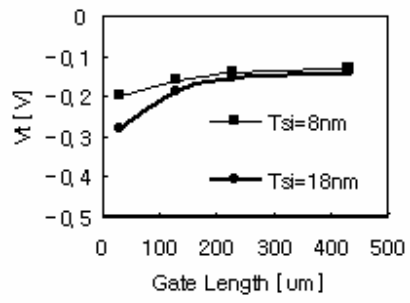

Fig. 5 Threshold voltage dependence on gate length (Lg) and body thickness (Tsi).

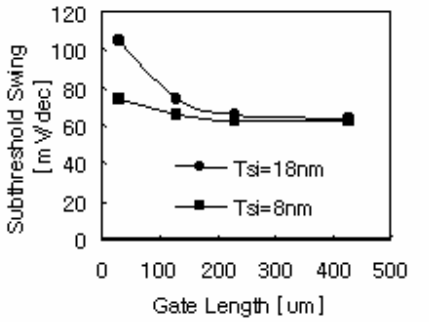

Fig. 6 Subthreshold swing dependence on gate length (Lg) and body thickness (Tsi).